

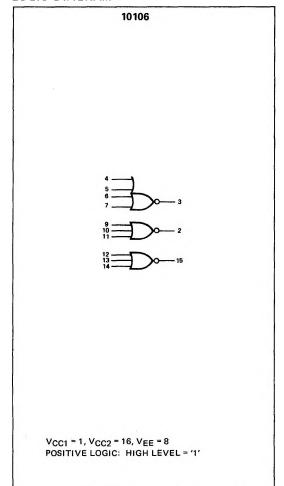
10106B,F: -30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10106 package contains one 4 input NOR gate and two 3 input NOR gates. The 10106 is optimized for high performance logic applications. The gate has an excellent speed power product of 50 picojoules. All inputs are terminated with a 50 k Ω resistor to VEE which eliminates the need to tie unused inputs low. The high impedance inputs and high output fanout is ideal for a transmission line environment. This gate meets the ECL 10,000 Series standard voltage, current and rise and fall time specifications.

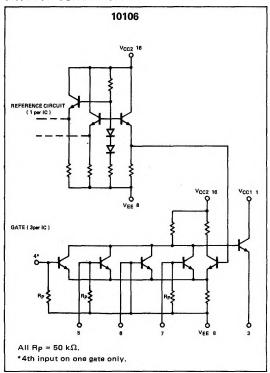
LOGIC DIAGRAM



FEATURES

- FAST PROPAGATION DELAY = 2.0 ns TYP
- LOW POWER DISSIPATION = 75 mW/PACKAGE TYP (NO LOAD)
- VERY HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS INTERNAL 50 k Ω PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIA-TIONS: VEE = -5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

CIRCUIT SCHEMATIC



TEMPERATURE RANGE

−30 to +85°C Operating Ambient

PACKAGE TYPE

B: 16-Pin Silicone DIP F: 16-Pin CERDIP

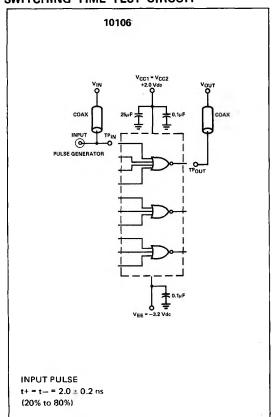
ELECTRICAL CHARACTERISTICS (at Listed Voltages and Ambient Temperatures).

	TEST VOLTAGE VALUES												
@ Test	(Volta)												
Temperature	VIH max	VIL min	VIHA min	VILA mek	VEE								
-30°C	-0.890	-1.890	-1.206	-1.500	-8.2								
+26°C	-0 810	-1.850	-1.106	-1,476	-5.2								
+86°C	-0.700	-1.825	-1.036	-1.440	-6.2								

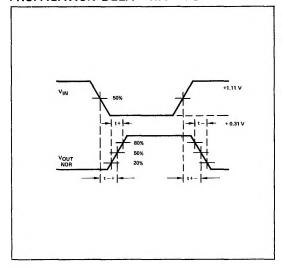
Characteristic Symbol		Pin	10106 Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:						
		Under tol Test	-30°C			+25° C		+85°C								(VCC)
	Symbol		Min	Max	Min	Тур	Max	Min	Max	Unit	VIH mex	VIL min	VIHA min	VILA max	VEE	Gnd
Power Supply Orein Current	1E	8	T -	_	I	15	21		Γ-	mAdc			T	_	8	1,16
	linH	4	-	-	-	-	266	-		μAdc	4	-	_	-	В	1,18
	InL	4	-	-	0.6	-	-	-	-	μAdc	-	4	-	-	8	1,18
Logic "1" Output Voltage VO	VOH	3	-1 060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc		4		-	8	1,16
		2	-1.060	-0.890	-0.960	_	-0.810	-0.890	-0.700			9	-			
Logic "0" Output Voltage VOL	VOL	3	-1.890	-1.675	-1.850	_	-1.650	-1.826	-1.616	Vdc	4	-	-	_	8	1,16
	_	2	-1.890	-1.875	-1.860	l – _	-1.650	-1.825	-1.616		9	-		L	L -	
Logic "1" Threshold Voltage V	VOHA	3	-1.080		-0.980	-	-	-0.910		Vdc	-		-	4	8	1,16
		2	-1.080		-0.980	_	1 -	-0.910				_			L - I	_
Logic "O" Threshold Valtege	VOLA	3	-	-1.656	_		-1.830	-	-1.696	Vdc	_	-	4	-	8	1,16
		2	-	-1.865	-	-	-1.630	-	-1.595		-	-	9	-	-	-
Switching Times *								Ì					Pulse In	Pulse Out	-3.2 V	+2.0 V
(50-ahm laed)			١,		1										\vdash	1.
Propagation Dalay	t4+ 3-	3	1.0	3.1	10	2.0	2.0	1.0	3.3	ns	-	-	4	3	8	1,16
	t4_ 3+	1	1.0	3.1	1.0	1 1	2.9	1.0	3.3	l ı	-	-	l i	1 1	lι	1 1
Riss Time (20% to 80%)	13+	l I	1.1	3.6	1.1	ΙL	3,3	1.1	3.7	ΙŢ	-	-	1 1		↓	i l
Fall Time (20% to 80%)	t3_	[🔻	1.1	3.6	1.1	1 7	33	1.1	3.7	1	l -	l -	, T	1		, ,

^{*}Unused outputs connected to a 50-ohm resistor to ground.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES:

- 1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
- 2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from $TP_{\rm in}$ to input pin and $TP_{\rm out}$ to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
- Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
- All voltage measurements are referenced to the ground terminal.
 Terminals not specifically referenced are left electrically open.