SCAS154A - D3715, NOVEMBER 1990 - REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Multiple Output Enables Allow Multiuser Control of the Interface
- Flow-Through Architecture Optimizes
 PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC[™] (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

This device contains eight flip-flops that feature 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

(TOP VIEW) OE1 OE2 27 OE3 1Q [2Q [26 1 1D 3 25 2D 3Q 🛮 4 4Q ∏ 5 24 🗍 3D GND [6 23 T 4D GND 7 22 V_{CC} GND **1**8 21 VCC GND [20 5D 9 5Q **1** 10 19**∏** 6D 6Q **1** 11 18 **∏** 7D 7Q [8D 12 17 8Q **CLKEN** 16 13 CLR I 15 T CLK 14

DW PACKAGE

With the clock-enable (CLKEN) input low, the eight edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. The 74ACT11825 has noninverting data (D) inputs. Taking the clear (CLR) input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-enable ($\overline{OE1}$, $\overline{OE2}$, and $\overline{OE3}$) inputs can be used to place the eight outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. The output enable (\overline{OE}) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74ACT11825 is characterized for operation from -40°C to 85°C.

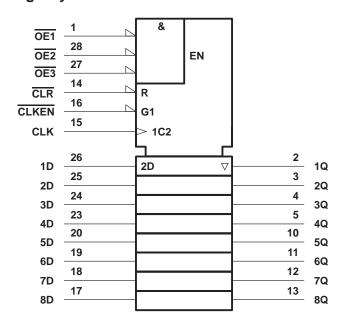
FUNCTION TABLE

	OUTPUT				
OE†	CLR	CLKEN	EN CLK D		Q
L	L	Х	Χ	Χ	L
L	Н	L	\uparrow	Н	Н
L	Н	L	\uparrow	L	L
L	Н	Н	Χ	Χ	Q_0
Н	Χ	X	Χ	Χ	Z

 $\dagger \overline{OE} = H$ if any of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are high. $\overline{OE} = L$ if all of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are low.

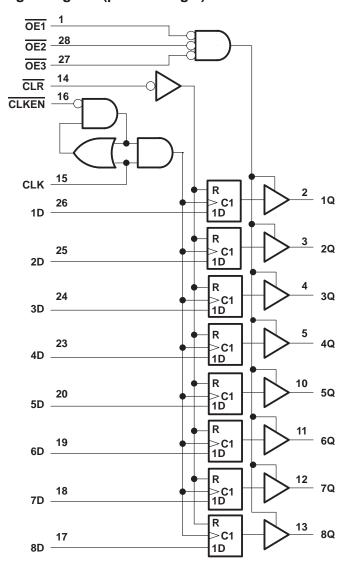
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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$).	±50 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC}) \dots$	±50 mA
Continuous current through V _{CC} or GND	±200 mA
Storage temperature range	–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			8.0	V
VI	Input voltage	0		VCC	V
VO	Output voltage	0		VCC	V
IOH	High-level output current			-24	mA
lOL	Low-level output current			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	ns/V
TA	Operating free-air temperature	-40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST COMPITIONS	١,,	T _A = 25°C				MAY	
PARAMETER	TEST CONDITIONS	vcc	MIN	TYP	MAX	MIN	0.1 0.44 0.44 1.65 ±1 ±5 80	UNIT
	Jan. 50 nA	4.5 V	4.4			4.4		
	$IOH = -50 \mu A$	5.5 V	5.4			5.4		
∨он	Jan. 24 mA	4.5 V	3.94			3.8		V
	IOH = -24 mA	5.5 V	4.94			4.8		
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V				3.85		
	504	4.5 V			0.1		0.1	1
	I _{OL} = 50 μA	5.5 V			0.1		0.1	
VOL	1 04 m A	4.5 V			0.36		0.44	V
	I _{OL} = 24 mA	5.5 V			0.36		0.44	
	$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V					1.65	
lį	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μΑ
loz	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	μΑ
Δl _{CC} ‡	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9		1	mA
C _i	$V_I = V_{CC}$ or GND	5 V		4.5		·		pF
Co	$V_O = V_{CC}$ or GND	5 V		12				pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

74ACT11825 8-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $\rm V_{CC}$ = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C					
		Γ		MAX	MIN	MAX	UNIT
fclock	Clock frequency		0	122	0	122	MHz
t _W	Dulas duration	CLR low	4		4		
	Pulse duration CLK high or low	4.5		4.5		ns	
	CLR inactiv	CLR inactive	3		3		
t _{su}	Setup time before CLK↑	Data	3		3		ns
		CLKEN high or low	3		3		
th	Hold time after CLKT Data CLKEN high or low	Data	1.5		1.5		20
		CLKEN high or low	2		2		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

	FROM	ТО	T _A = 25°C					
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
f _{max}			122			122		MHz
^t PLH	CLK	_	4.6	7.7	10.2	4.6	11.6	
t _{PHL}		Q	5.1	8.4	10.9	5.1	12.3	ns
tPHL	CLR	Q	4.5	8.5	11.9	4.5	13.2	ns
^t PZH		_	3.3	6.4	9.2	3.3	10.4	
^t PZL	ŌĒ	Q	4.2	7.9	11.5	4.2	13	ns
^t PHZ	ŌĒ	_	6.1	8.5	10.7	6.1	12	
tPLZ		Q	5.5	7.9	10	5.5	11.2	ns

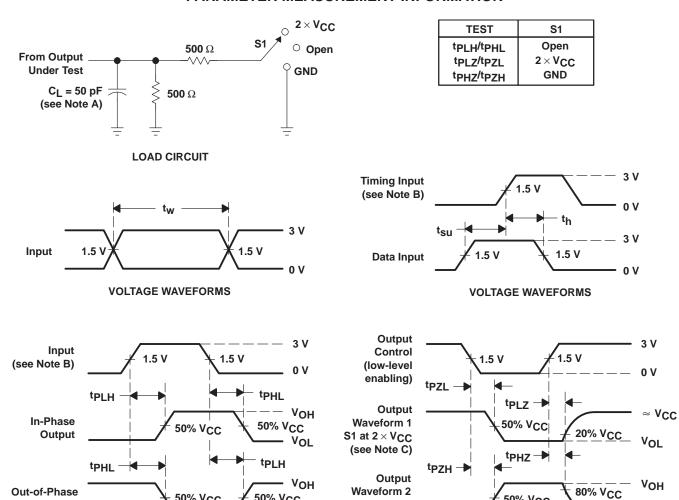
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CON	TYP	UNIT		
C _{pd} Power dissipation capacitance	Device dissination consistence	Outputs enabled	0 50 -5	4 4 MILE	47	
	Outputs disabled	$C_L = 50 \text{ pF},$	f = 1 MHz	34	pF	

50% V_CC

VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

Output

50% V_{CC}

VOLTAGE WAVEFORMS

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} = 3 \text{ ns}$, $t_{f} = 3 \text{ ns}$.

S1 at GND

(see Note C)

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

50% V_CC

 v_{OL}

Figure 1. Load Circuit and Voltage Waveforms

≈ 0 V

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