CYPRESS

CY54/74FCT191T

4-Bit Up/Down Binary Counter

Features

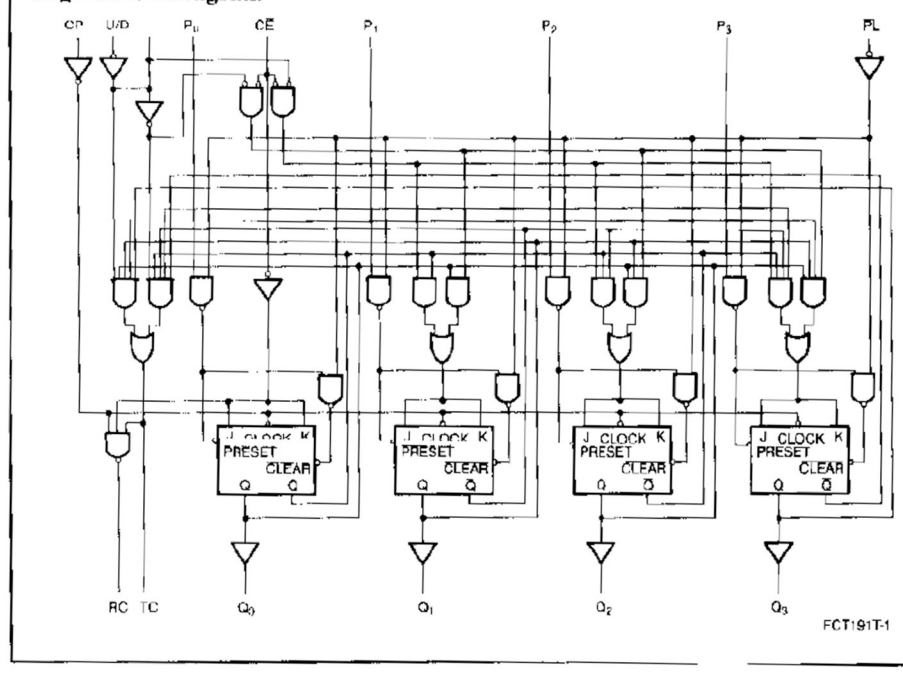
- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 6.2 ns max. (Com'l) FCT-A speed at 7.8 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l), 32 mA (Mil)
  Source current 32 mA (Com'l), 12 mA (Mil)
- Three-State outputs

Functional Description

The FCT191T is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting. The preset allows the FCT191T to be used in programmable dividers. The count enable input, terminal count output, and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

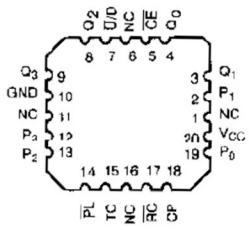
Logic Block Diagram



FCT191T-1

Pin Configurations

LCC
Top View



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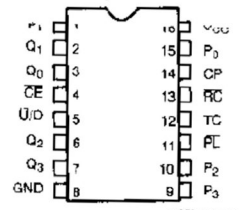
DIP/SOIC/QSOP
Top View



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Pin Description

Name	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}$/D	Up/Down Count Control Input
Q	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output

$\overline{RC}$ Function Table[1]

Inputs		Outputs	
$\overline{CE}$	CP	T[2]	$\overline{RC}$
L	⌝⌜	H	⌝⌜
H	X	X	H
X	X	L	H

Mode Select[1]

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌜	Count Up
H	L	H	⌜	Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −65°C to +135°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Output Voltage ..... −0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .... 120 mA

Power Dissipation 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	−40°C to +85°C	5V ± 5%
Military[5]	All	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[6]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=−15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=−12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[7]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA			−0.7	−1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[8]	V_{CC}=Max., V_{OUT}=0.0V		−60	−120	−225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[7]

Parameter	Description	Typ.[6]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ⌜ = LOW-to-HIGH clock transition. ⌞⌟ = Low Pulse.
2. TC is generated internally.
3. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. T_A is the "instant on" case temperature.
6. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
7. This parameter is guaranteed but not tested.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT191T				FCT191AT				Unit	Fig. No.[14]
		Military		Commercial		Military		Commercial			
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	1.5	16.0	1.5	12.0	1.5	10.5	1.5	7.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	2.0	16.0	1.5	14.0	2.0	12.2	1.5	11.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$	1.5	12.5	1.5	8.5	1.5	10.0	1.5	8.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	2.0	8.5	1.5	8.0	2.0	8.0	1.5	7.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay U/D to $\overline{RC}$	4.0	22.5	1.5	20.0	4.0	14.7	1.5	13.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{TC}$	3.0	13.0	1.5	11.0	3.0	8.5	1.5	7.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{Q}_n$	1.5	16.0	1.5	14.0	1.5	10.4	1.5	9.1	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{Q}_n$	3.0	14.0	2.0	13.0	3.0	9.1	2.0	8.5	ns	1, 5
t_{SU}	Set-Up Time HIGH or LOW P_n to $\overline{PL}$	6.0		5.0		5.0		4.0		ns	4
t_H	Hold Time HIGH or LOW P_n to $\overline{PL}$	1.5		1.5		1.5		1.5		ns	4
t_{SU}	Set-Up Time LOW $\overline{CE}$ to CP	10.5		10.0		9.5		9.0		ns	4
t_H	Hold Time LOW $\overline{CE}$ to CP	0		0		0		0		ns	4
t_{SU}	Set-Up Time HIGH or LOW $\overline{U}$/D to CP	12.0		12.0		10.0		10.0		ns	4
t_H	Hold Time HIGH or LOW $\overline{U}$/D to CP	0		0		0		0		ns	4
t_W	$\overline{PL}$ Pulse Width LOW	8.5		6.0		8.0		5.5		ns	5
t_W	Clock Pulse Width[6] HIGH or LOW	7.0		5.0		6.0		4.0		ns	5
t_{RFM}	Recovery Time $\overline{PL}$ to CP	7.5		6.0		6.5		5.0		ns	6

Notes:
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. See "Parameter Measurement Information" in the General Information Section.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[6]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[9] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[10]	V_{CC}=Max., One Bit Toggling, Preset Mode, 50% Duty Cycle, Outputs Open, $\overline{MR}=V_{CC}=\overline{SR}$, $\overline{PL}=\overline{CE}=\overline{U}/D=CP=GND$, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[11]	V_{CC}=Max., Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{PL}=\overline{CE}=\overline{U}/D=CP=GND$, $V_{IN}=V_{CC}$, V_{IN}=GND	0.4	0.8	mA
		V_{CC}=Max., Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, V_{IN}=3.4V or V_{IN}=GND	0.7	1.8	mA
		V_{CC}=Max., Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=5 MHz, $\overline{PL}=\overline{CE}=\overline{U}/D=CP=GND$, $V_{IN}=V_{CC}$, V_{IN}=GND	1.3	2.6[12]	mA
		V_{CC}=Max., Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=5 MHz, $\overline{PL}=\overline{CE}=\overline{U}/D=CP=GND$, V_{IN}=3.4V or V_{IN}=GND	2.3	6.6[12]	mA

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_iN_i)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_i = Input signal frequency
    N_i = Number of inputs changing at f_i
    All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	FCT191CT				Unit	Fig. No.[14]
		Military		Commercial			
		Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	1.5	8.4	1.5	6.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to TC	1.5	9.8	1.5	9.4	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$	1.5	7.9	1.5	6.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	1.5	6.4	1.5	6.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	2.5	11.7	1.5	11.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC	1.5	6.8	1.5	6.1	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	1.5	8.3	1.5	7.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	2.0	7.3	2.0	7.2	ns	1, 5
t_{SU}	Set-Up Time, HIGH or LOW, P_n to $\overline{PL}$	4.0		3.5			4
t_H	Hold Time, HIGH or LOW, P_n to $\overline{PL}$	1.5		1.0		ns	4
t_{SU}	Set-Up Time LOW, $\overline{CE}$ to CP	7.6		7.2		ns	4
t_H	Hold Time LOW, $\overline{CE}$ to CP	0		0		ns	4
t_{SU}	Set-Up Time, HIGH or LOW, $\overline{U}$/D to CP	8.5		8.0		ns	4
t_H	Hold Time, HIGH or LOW, $\overline{U}$/D to CP	0		0		ns	4
t_W	PL Pulse Width LOW	6.0		5.0		ns	5
t_W	Clock Pulse Width[6] HIGH or LOW	5.0		4.0		ns	5
t_{REM}	Recovery Time $\overline{PL}$ to CP	5.0		4.5		ns	6

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.2	CY74FCT191CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT191CTQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT191CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
8.4	CY54FCT191CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT191CTLMB	L61	20-Pin Square Leadless Chip Carrier	
7.8	CY74FCT191ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT191ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT191ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
10.5	CY54FCT191ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT191ATLMB	L61	20-Pin Square Leadless Chip Carrier	
12.0	CY74FCT191TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT191TQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT191TSOC	S1	16-Lead (300-Mil) Molded SOIC	
16.0	CY54FCT191TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT191TLMB	L61	20-Pin Square Leadless Chip Carrier	

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