National Semiconductor

PRELIMINARY

74LCX652
Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, $\overline{OEBA}$) are provided to control the transceiver function.

The LCX652 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

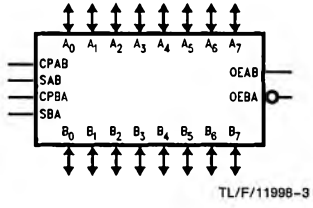
The LCX652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 Series 652
- Latchup performance exceeds 300 mA
- ESD performance:
  Human Body Model >2000V
  Machine/Model >250V

Ordering Code: See Section 11

Logic Symbols



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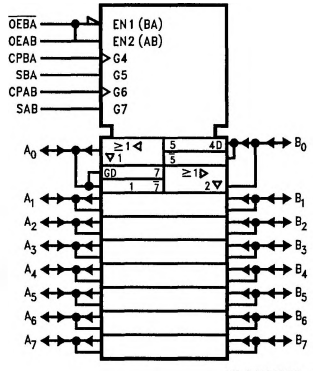
IEEE/IEC



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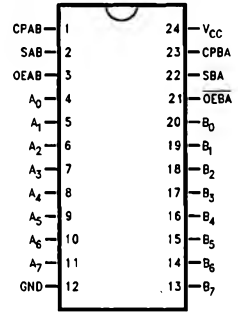
Connection Diagram

Pin Assignment for SOIC and TSSOP



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Pin Names	Description
A_0–A_7, B_0–B_7	A and B Inputs/TRI-STATE® Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

	SOIC JEDEC	TSSOP JEDEC
Order Number	74LCX652WM 74LCX652WMX	74LCX652MTCX
See NS Package Number	M24B	MTC24

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

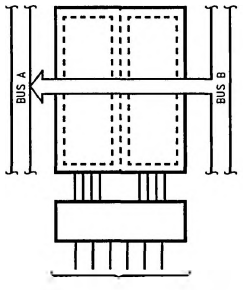
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Real-Time Transfer
Bus B to Bus A



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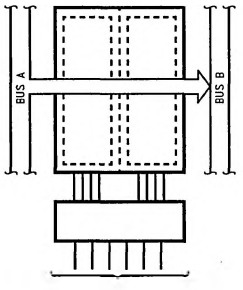
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus A to Bus B



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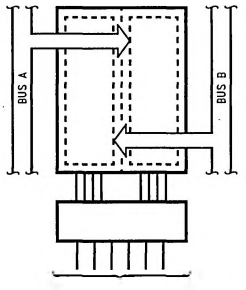
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Storage



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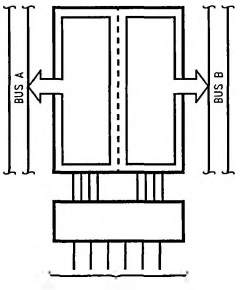
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
X	H	↓	X	X	X
L	X	X	↓	X	X
L	H	↓	↓	X	X

Transfer Storage
Data to A or B



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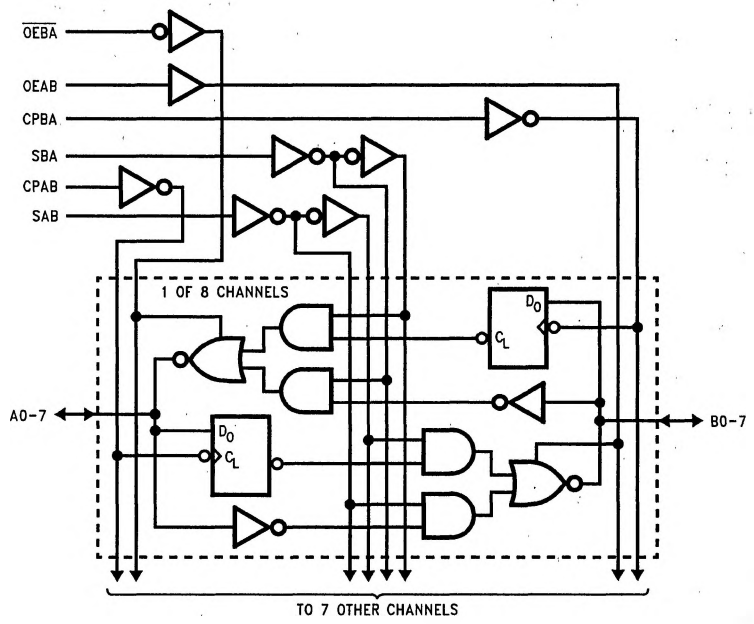
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FIGURE 1

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table (Note)

Inputs						Inputs/Outputs		Operating Mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_0 thru A_7	B_0 thru B_7	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Not Specified	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW to HIGH Clock Transition

Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
Output Voltage (V_O)	
Outputs TRI-STATE	−0.5V to +7.0V
Outputs Active (Note 2)	−0.5V to V_{CC} + 0.5V
DC Input Diode Current (I_{IK}) (V_I) < 0	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *I_O Absolute Maximum Ratings must be observed.*

Recommended Operating Conditions

Supply Voltage	
Operating	2.0V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage (V_I)	0.0V to 5.5V
Output Voltage (V_O)	
Output in Active State	0.0V to V_{CC}
Output in "OFF" State	0.0V to 5.5V
Output Current I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	
V_{CC} = 2.7V to 3.0V	
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C		Units	Conditions
			Min	Max		
V_{IH}	High Level Input Voltage	2.7–3.6	2.0		V	V_{OUT} ≤ 0.1V or ≥ V_{CC} − 0.1V
V_{IL}	Low Level Input Voltage	2.7–3.6		0.8		
V_{OH}	High Level Output Voltage	2.7–3.6	V_{CC} − 0.2		V	I_{OH} = −100 μA
		2.7	2.2			I_{OH} = −12 mA
		3.0	2.4			I_{OH} = −18 mA
		3.0	2.2			I_{OH} = −24 mA
V_{OL}	Low Level Output Voltage	2.7–3.6		0.2	V	I_{OL} = 100 μA
		2.7		0.4		I_{OL} = 12 mA
		3.0		0.55		I_{OL} = 24 mA
I_I	Input Leakage Current	2.7–3.6		±5.0	μA	0 ≤ V_I ≤ 5.5V
I_{OZ}	TRI-STATE I/O Leakage	2.7–3.6		±5.0	μA	0 ≤ V_O ≤ 5.5B V_I = V_{IH} or V_{IL}
I_{OFF}	Power Off Leakage Current	0		100	μA	V_I or V_O = 5.5V
I_{CC}	Quiescent Supply Current	2.7–3.6		10	μA	V_I = V_{CC} or GND
				±10	μA	3.6 ≤ (V_I, V_O) ≤ 5.5V
ΔI_{CC}	Increase in I_{CC} per Input	2.7–3.6		500	μA	V_{IH} = V_{CC} − 0.6V

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC}, (V)	$T_A = +40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Max (Note 2)	
t_{PHL}, t_{PLH}	Propagation Delay Clock to Bus	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PHL}, t_{PLH}	Propagation Delay Bus to Bus	2.7 3.0–3.6	1.5 1.5	8.0 7.0	ns
t_{PHL}, t_{PLH}	Propagation Delay SAB or SBA to A or B	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PZH}, t_{PZL}	Output Enable Time OEBA to A	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time OEBA to A	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PZH}, t_{PZL}	Output Enable Time OEBA to A	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time OEAB to B	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_S	Setup Time Bus to Clock	2.7 3.0–3.6	2.5 2.5		ns
t_H	Hold Time Bus to Clock	2.7 3.0–3.6	1.5 1.5		ns
t_W	Clock Pulse Width	2.7 3.0–3.6	4.0 4.0		ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)	3.0		1.0	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics See Section 0 for Test Methodology

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Typical	Units	Conditions
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$V, $V_{IL} = 0$V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$V, $V_{IL} = 0$V

Capacitance

Symbol	Parameter	Typical	Units	Conditions
C_{IN}	Input Capacitance	7	pF	V_{CC} = Open $V_I = 0$V or V_{CC}
$C_{I/O}$	Input/Output Capacitance	8	pF	$V_{CC} = 3.3$V $V_I = 0$V or V_{CC}
C_{PD}	Power Dissipation Capacitance	32	pF	$V_{CC} = 3.3$V $V_I = 0$V or V_{CC} F = 10 MHz