signetics

BUFFER REGISTERS

N,F,Q PACKAGES

DIGITAL 8000 SERIES TTL/MSI

8200
8201
8202
8203

DESCRIPTION

The 8200/8201/8202/8203 MSI Buffer Registers are arrays of ten clocked "D" flip-flops especially suited for parallel-in parallel-out register applications. They are also suitable for general purpose applications as parallel-in serial-out, serial-in parallel-out registers.

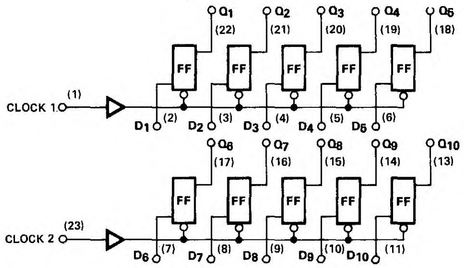
The flip-flops are arranged as dual 5 arrays, (8200 & 8201) and single 10 arrays with reset, (8202 & 8203). The true output of each bit is made available to the user.

The 8200 and 8202 feature true "D" inputs. The logic state presented at these "D" inputs will appear at the Q outputs after a negative transition of the clock.

The 8201 and 8203 feature complementing "D" inputs ("$\overline{D}$"). The logic state presented at these "$\overline{D}$" inputs will invert and appear at the Q outputs after a negative going transition of the clock. This complementing input feature ("$\overline{D}$") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

LOGIC DIAGRAMS AND TRUTH TABLES

DUAL 5-BIT BUFFER REGISTER

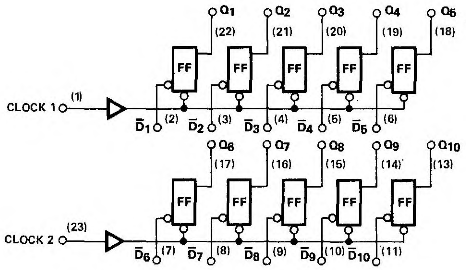


D_n	Q_{n+1}
1	1
0	0

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8200

DUAL 5-BIT BUFFER REGISTER—INVERTED INPUTS

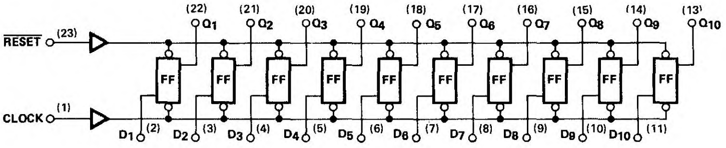


$\overline{D}_n$	Q_{n+1}
1	0
0	1

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8201

10-BIT BUFFER REGISTER



D_n	$\overline{\text{RESET}}$	Q_{n+1}
1	1	1
0	1	0

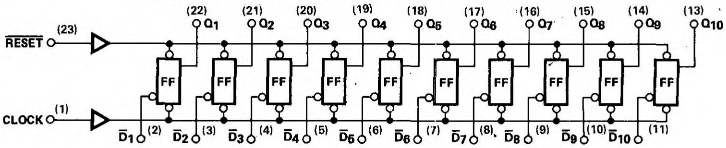
$\overline{\text{RESET}} = 0 \Rightarrow Q = 0$
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8202

LOGIC DIAGRAMS AND TRUTH TABLES (Cont'd)

10-BIT BUFFER REGISTER–INVERTED INPUTS



D_n	$\overline{\text{RESET}}$	Q_{n+1}
0	1	1
1	1	0

$\overline{\text{RESET}}$ = 0 → Q = 0
(OVERRIDES CLOCK)
n IS TIME PRIOR TO CLOCK
n+1 IS TIME FOLLOWING CLOCK

V_{CC} = (24)
GND = (12)
( ) = Denotes Pin Numbers

8203

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	D_n 8200 8202	$\overline{D}_n$ 8201 8203	CLOCK	$\overline{\text{RESET}}$ 8202 8203	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	2.0V	0.8V	Pulse		– 800µA	6
"0" Output Voltage			0.4	V	0.8V	2.0V	Pulse		9.6mA	7
"0" Input Current										
D_n(8200, 8202)	-0.1		-1.6	mA	0.4V					
$\overline{D}_n$(8201, 8203)	-0.1		-1.6	mA		0.4V				
Clock	-0.1		-1.6	mA			0.4V			
$\overline{\text{Reset}}$ (8202, 8203)	-0.1		-1.6	mA				0.4V		
"1" Input Current										
D_n (8200, 8202)			40	µA	4.5V					
$\overline{D}_n$ (8201, 8203)			40	µA		4.5V				
Clock			40	µA			4.5V			
Reset (8202, 8203)			40	µA				4.5V		
Input Voltage Rating (All inputs)	5.5			V	10mA	10mA	10mA	10mA		
Power/Current Consumption		409/77.7	580/110	mW/mA	0V	0V	0V			11,13

T_A = 25°C and V_{CC} = 5.0V

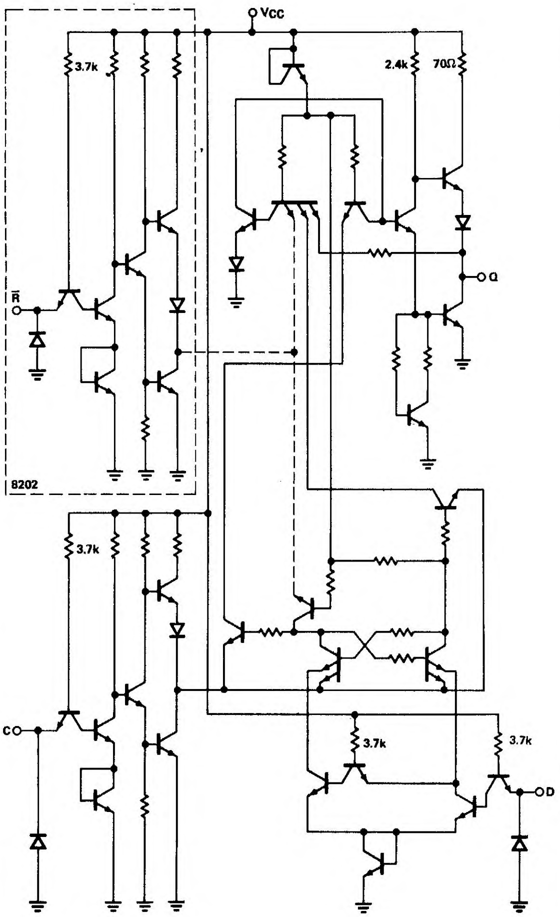
CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Propagation Delay						
t_{on} Clock to Q		30	45	ns		8
t_{off} Clock to Q		25	40	ns		8
t_{on} Reset to Q		30	45	ns		8
Set Up Time		6	15	ns		10
Hold Time		0	5	ns		12
Minimum Clock Pulse Width		12	17	ns		
Transfer Rate	15	35		MHz		8
Output Short Circuit Current	-20		-70	mA		9, 13

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are tied to V_{CC}.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Not more than one output should be shorted at a time.
10. Set Up Time defined as data presence before clock.
11. Outputs are in the low state for this test.
12. Hold time defined as data presence after clock.
13. V_{CC} = 5.25 volts.

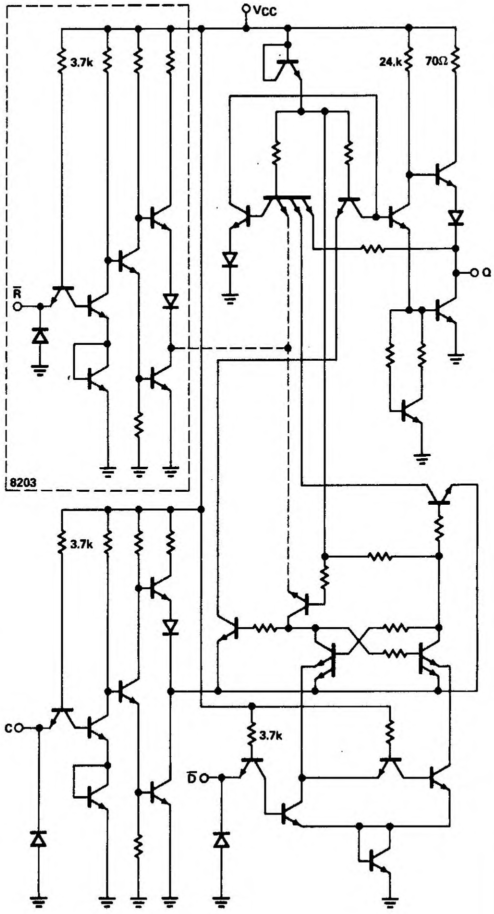
SCHEMATIC DIAGRAMS

DUAL 5-BIT BUFFER REGISTER 8200
SINGLE 10-BIT BUFFER REGISTER 8202



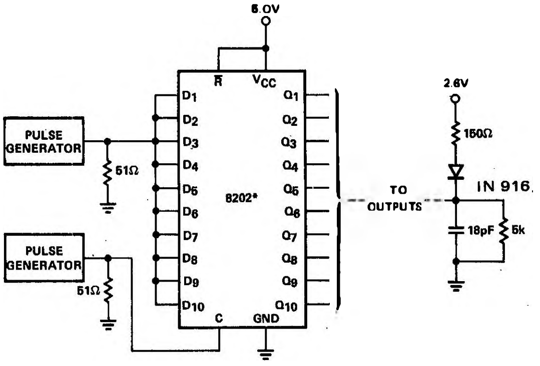
DUAL 5-BIT BUFFER REGISTER
INVERTED INPUTS 8201

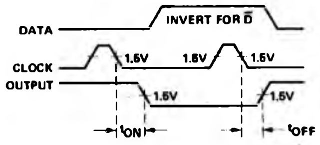
SINGLE 10-BIT BUFFER REGISTER
INVERTED INPUTS 8203



AC TEST FIGURES AND WAVEFORMS

t_{pd} FROM CLOCK TO Q

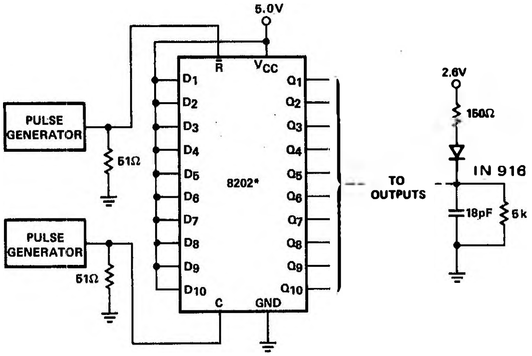


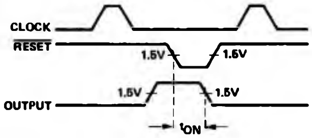


INPUT PULSE:
Data = P.R.R. = 7.5 MHz
Clock = P.R.R. = 15 MHz
PW = 17 ns (at 50% point)
$t_r = t_f = 5$ ns Max.
Amplitude = 2.6V.

*Refer to the Pin-Outs for the 8200/01/03 AC Testing.

t_{on} FROM $\overline{\text{RESET}}$ TO Q



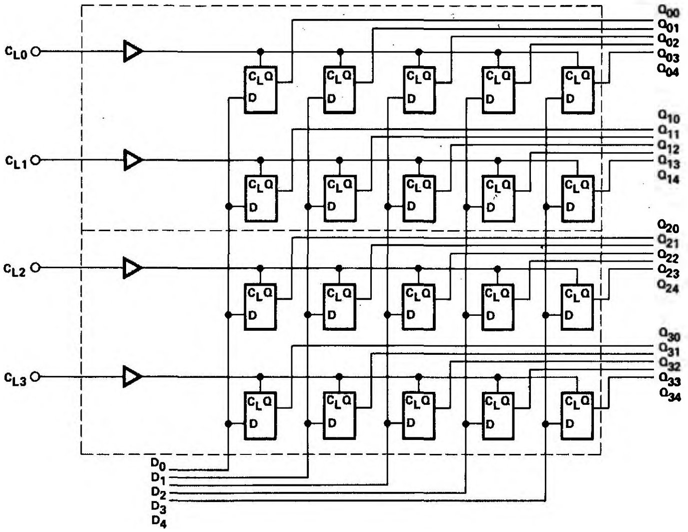


INPUT PULSE:
Amplitude = 2.6V
Clock: P.R.R. = 5 MHz
$\overline{\text{Reset}}$: P.R.R. = 5 MHz
PW = 30 ns (at 50% point)
$t_r = t_f = 5$ ns

*Refer to the Pin-Outs for the 8200/01/02/03 AC Testing.

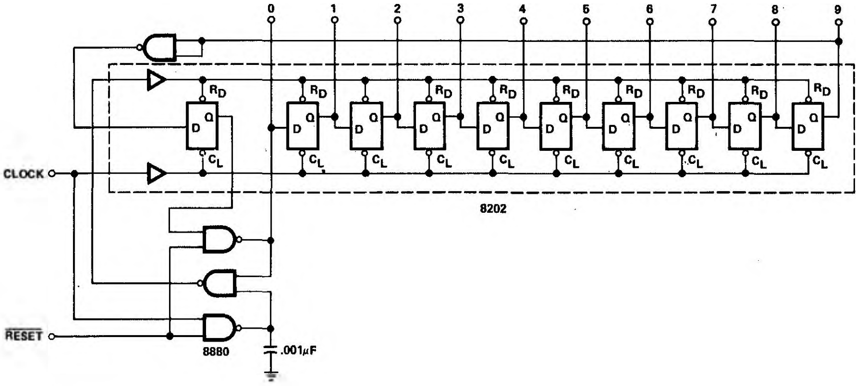
TYPICAL APPLICATIONS

20 BIT (4 WORDS X 5 BITS EACH) MEMORY CELL



Total Package Count = 2-8200's

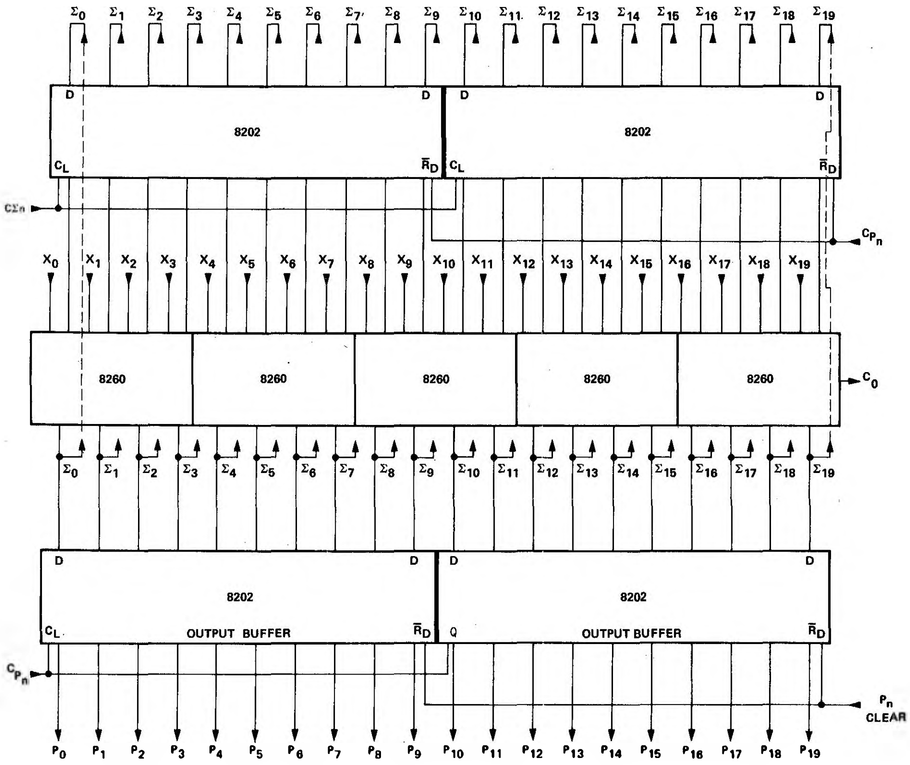
ONE OUT OF TEN – COUNTER/DISPLAY (SELF-CORRECTING)



Total Package Count = 1-8202; 1-8880

TYPICAL APPLICATIONS (Cont'd)

MULTIPLICATION AT 10MHz OF A 20-BIT BINARY WORD



$P_n = (X_n)M$ WHERE $X_n \equiv$ MULTIPLICAND

$M \equiv$ MULTIPLIER

TOTAL PACKAGE COUNT = 9 PACKAGES (4-8202'S AND 5-8260'S)