

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8220 CAM Element is a high speed monolithic array, incorporating the necessary addressing logic and eight identical memory cells organized as four words, each being two bits long. In reference to data-in/data-stored, the 8220 can be conditioned to perform the following functions: associate, write-in only, and read-out only.

When addressed into the "ASSOCIATE" mode, this element offers the novel capability of data association, where each cell (M_{nj}) will respond with a "Match" or "Mismatch" answer (Y_n) to each bit presented to the data inputs (I_j), depending on presence or absence of an alike bit stored within the cell.

Write-in can be simultaneously done to all bits, or one bit at a time. Read-out of stored information is performed on

one word at a time. Cell-selection for read and write is performed by proper addressing of Y_n and A_n lines.

The element's output structures (Y_n and D_j) are of the "bare collector" variety and can be mutually connected, thus allowing direct expansion when multiple packages are employed. Expansion of the CAM may be implemented in both directions, i.e., in the word length and in the number of words.

The CAM circuit structure is the familiar TTL type (DCL Family) and fully compatible with TTL and DTL input/output structures.

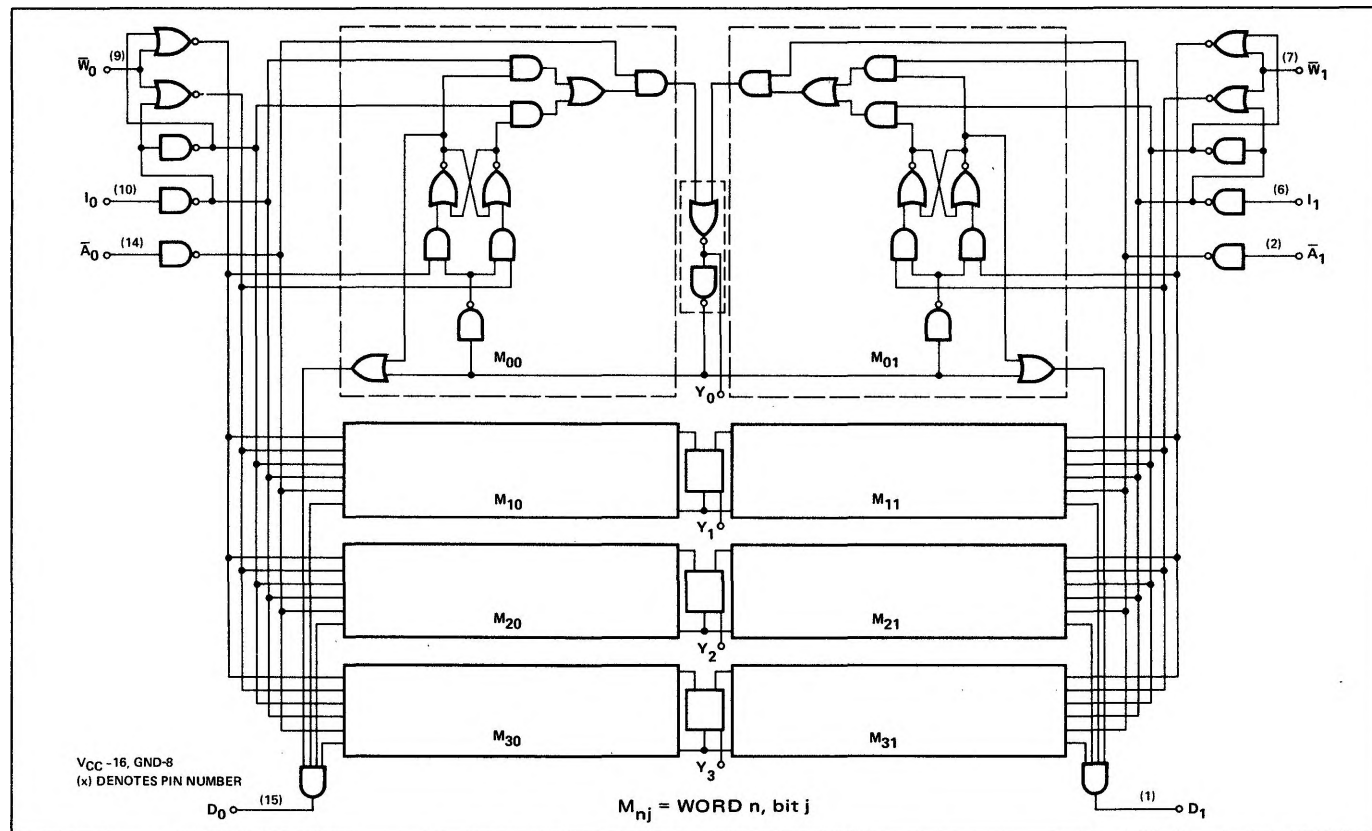
FEATURES

- WRITE ENABLE CONTROL LINES
- ASSOCIATE CONTROL LINES
- ADDRESS SELECT CONTROL LINES
- ASSOCIATES IN 20nsec TYP.
- 16 PIN PACKAGE (1/3 SIZE OF 24 PIN PACKAGE)
- OPEN COLLECTOR OUTPUTS
- DIODE PROTECTED INPUTS

APPLICATIONS

- DATA-TO-MEMORY COMPARISON
- PATTERN RECOGNITION
- HIGH SPEED INFORMATION RETRIEVAL
- CACHE MEMORY
- AUTO CORRELATION
- VIRTUAL MEMORY
- LEARNING MEMORY

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				Wj	Aj	Ij	Yi	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
"0" Output Voltage											
Yn			0.4	V	2.0V	0.8V	2.0V	30mA			8, 9
			0.6	V	2.0V	0.8V	2.0V	60mA			
Dj			0.4	V	2.0V	2.0V			0.8V	20mA	8, 9
			0.6	V	2.0V	2.0V			0.8V	40mA	
"1" Output Leakage Current											
Yn			125	μA		2.0V					10
Dj			100	μA				0V	0V		10
"1" Input Current											
Ij and Aj			40	μA		4.5V	4.5V				
Wj			80	μA	4.5V						
"0" Input Current											
Ij, Yn and Aj	-0.1		-1.2	mA		0.4V	0.4V	0.4V			

 $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{V}$

CHARACTERISTICS	LIMITS				Wj	Aj	Tj	Yi	Yk	Dj	NOTES
	MIN.	TYP.	MAX.	UNITS							
Delay Time											
Associate (Aj to Yn)		20	30	ns							8, 11
Associate (Ij to Yn)		35		ns							8, 11
Read-Out (Yn to Dj)		30		ns							8, 11
Write-In to Read-Out (Wj to Dj)		30		ns							
Write Pulse Width		30		ns							
Power Consumption			590	mW							

NOTES:

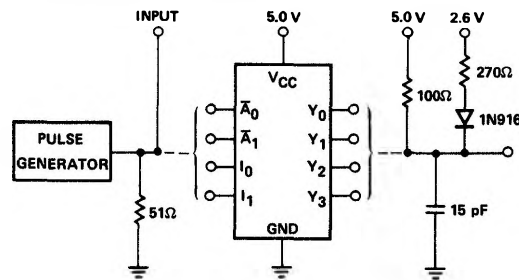
- All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current is defined as into the terminal referenced.
- Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Measurements apply to each gate element independently.
- Manufacturer reserves the right to make design and process changes and improvements.
- Prior to this test write in a "0" in all or desired Memory cells as follows: $Wj = Ij = 0V$, $Aj = V_{CC}$.
- Output sink current is supplied through a resistor to V_{CC} .
- Connect an external 1K ohm + 1% resistor from V_{CC} to the output terminal for this test.
- See AC test Figures on the following pages.

MODE OF OPERATION

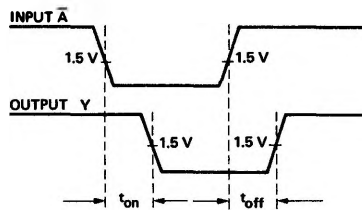
FUNCTION	$\overline{W}_0 \overline{W}_1 \overline{A}_0 \overline{A}_1 I_0 I_1$	REMARKS (Ref. Definitions & Glossary)	FUNCTION	$\overline{W}_0 \overline{W}_1 \overline{A}_0 \overline{A}_1 I_0 I_1$	REMARKS (Ref. Definitions & Glossary)
HOLD	1 1 1 1 x x	NO OPERATION	HOLD	1 1 1 1 x x	NO OPERATION
ASSOCIATE	1 1 1 0 x x	<p>Output State</p> <p>Question Answer</p> <p>$I_1 = M_{i1}$?</p> <p>YES — $Y_i = 1, Y_k = 0$</p> <p>NO — $Y_i = Y_k = 0$</p>	WRITE-IN	1 0 1 1 x x	<p>Forced</p> <p>$Y_i \quad Y_k$</p> <p>1 0</p> <p>WRITE I_1 into M_{i1}</p>
	1 1 0 1 x x	<p>$I_0 = M_{i0}$?</p> <p>YES — $Y_i = 1, Y_k = 0$</p> <p>NO — $Y_i = Y_k = 0$</p>		0 1 1 1 x x	<p>1 0</p> <p>WRITE I_0 into M_{i0}</p>
	1 1 0 0 x x	<p>$I_1 = M_{i1}$ and $I_0 = M_{i0}$?</p> <p>YES — $Y_i = 1, Y_k = 0$</p> <p>NO — $Y_i = Y_k = 0$</p>		0 0 1 1 x x	<p>1 0</p> <p>WRITE I_1 and I_0 into M_{i1} and M_{i0}</p>
READ-OUT			READ-OUT	1 1 1 1 x x	<p>1 0</p> <p>$D_0 = 1$ - IF $M_{i0} = 1$ 0 - IF $M_{i0} = 0$</p>
				1 1 1 1 x x	<p>1 0</p> <p>$D_1 = 1$ - IF $M_{i1} = 1$ 0 - IF $M_{i1} = 0$</p>
				1 1 1 1 x x	<p>0 0</p> <p>$D_0 = D_1 = 1$</p>

AC TEST FIGURES AND WAVEFORMS

ASSOCIATE DELAY AND INPUT DELAY



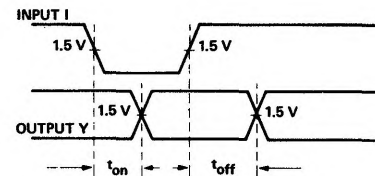
ASSOCIATE DELAY



NOTES:

- When checking \overline{A}_0 let $\overline{A}_1 = "1"$ and when checking \overline{A}_1 let $\overline{A}_0 = "1"$.
- $\overline{W}_0 = \overline{W}_1 = "1"$.

INPUT DELAY

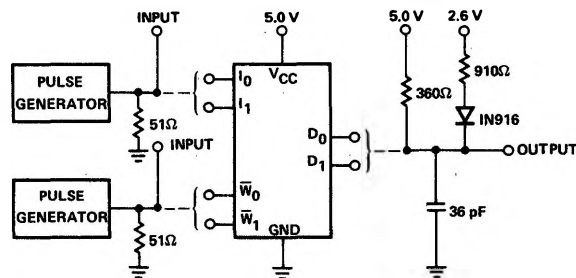


NOTES:

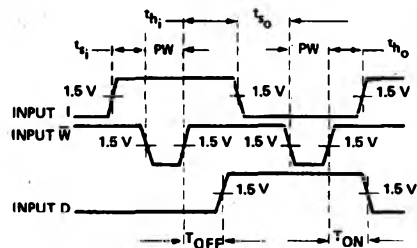
- When checking I_1 , $\overline{A}_1 = "0"$ and $\overline{A}_0 = "1"$ and when checking I_0 , $\overline{A}_0 = "0"$ and $\overline{A}_1 = "1"$.
- $\overline{W}_0 = \overline{W}_1 = "1"$.

AC TEST FIGURES AND WAVEFORMS (Cont'd)

WRITE DELAY



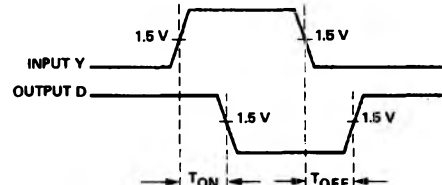
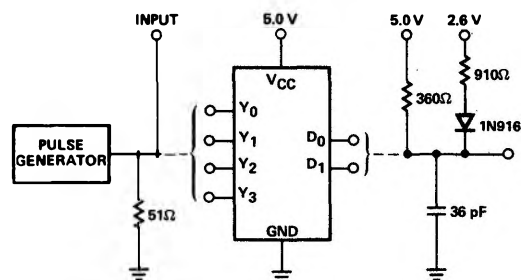
t_{sj} = "1" set-up time.
 t_{so} = "0" set-up time.
 t_{hj} = "1" hold time.
 t_{ho} = "0" hold time.
 PW = Pulse width



NOTES:

1. $A_0 = A_1 = "1"$.
2. Let all non-selected Y's = "0".
3. W's pulse width is 40ns @50% points.

READ DELAY



NOTES:

1. A tested bit must store a "0".
2. $\overline{W}_0 = \overline{W}_1 = "1"$.
3. $A_0 = A_1 = "1"$.
4. All non-tested Y's = "0".

GENERAL NOTES FOR AC TESTING:

1. Use 5k Probes for all AC tests TEK 169 or equivalent.
2. The Pulse Generator signal should consist of the following
 Frequency: 10 MHz \pm 5 MHz
 Amplitude: 0V to 3V
 Rise & Fall Times: 5 ns \pm 2ns
3. i = bit number (i = 0, 1). j = word number (j = 0, 1, 2, 3).

INPUT/OUTPUT DEFINITIONS

 I_j - Data Inputs

Data entering these terminals are either compared with stored information at the cell(s) in the "associate" mode or stored in the cell(s) in the "write-in" mode.

 \overline{A}_j - Associate Controls

A logical "0" at this pin enables Data-Cell association to result into a defined logical level at the Y_n lines (e.g. $Y_n = "1"$ = Match, $Y_n = "0"$ = Mismatch). A logical "1" at this pin forces all Y_n to a "1".

 \overline{W}_j - Write Enable

A logical "0" at this control pin opens the gates of the selected word, allowing data-in to be stored. A logical "1" locks the gates such that data-in can no longer disturb the cell(s).

 Y_n - "Associate" Output and Address Selection Control

During "Associate" mode these "bare collector" lines provide output results of match or mismatch between input and stored

data (logical "1" = Match, logical "0" = Mismatch).

In the read and write modes these terminals act as input controls and word-select lines Y lines (Y_1) associated with words desired to accept writing of data or read-out are to be kept in the logical "1" state and the remaining Y lines (Y_k) to be forced to a logical "0" state. (Note that $A = 1$ forces all $Y_n = 1$).

 D_j - Data Output

These are "bare collector" output lines indicating the state of one or more selected cells. Cell-Selection is accomplished as defined under " Y_n " above.

GLOSSARY OF TERMS - SUBSCRIPTS

A. n = Word number = 0, 1, 2 and 3

j = Bit number = 0 or 1

i = Input/Output number(s) associated with cell(s) upon which a "Write-in", "Read-out" or other function is being performed.

k = Input/Output number(s) other than "i" above.

M = Designation of Memory Cell (word) = eight identical cells in each package.

B. Examples

1. I_j for bit "1" equals I_1 .

2. $M_{nj} = M_{10}$ = word "1" bit "0".

3. $Y_i = 0, Y_k = 1$: for i = words 1 and 3; then k = words 0 and 2: $Y_{1,3} = 0$ and $Y_{0,2} = 1$.

APPLICATION: LEARNING MEMORY

Description: This system is a CAM array with peripheral IC circuitry designed to operate as a learning memory. It is organized in two sections of equal capacity, the total memory size (both sections) being 8 ten bit words. Either section can be selected through the section SELECT line, and the memory is easily expandable in the number of words and in word length.

By activating the COMPARE line, a new word is loaded into the buffer and is presented to the memory. Through the novel feature of data association, which is unique with CAM elements, the buffer's content is compared with the words stored in memory. If the input word, with which the memory was presented, is already contained in storage, no need for "learning," i.e. data acquisition, exists. This fact is indicated by a match from one of the Y_n lines ($Y_i = 1$) and thus no write command is initiated.

However, if a word is loaded into the buffer register and it is not contained in the selected memory section, a write cycle must be initiated. The memory has to "learn" i.e. put the word into storage. Since the CAM array is normally in the ASSOCIATE mode, no match could have occurred between the word TO BE LEARNED in the buffer and the words already in storage. In response to this situation, all

Y_n outputs will be equal to "0". The NOR gate output will now change to a "1". By the use of appropriate gating circuitry, the WRITE line will be enabled in the selected memory section.

Before a WRITE operation is initiated, a location select has to be made such that the word to be written into the memory will go to the proper place. For this reason, a tag CAM is employed to keep track of memory locations, both empty and full. When a word is written into memory, a "1" is simultaneously written into the tag CAM. Thus, it is possible to keep track of the filled memory locations.

In particular, the memory is always in the ASSOCIATE mode when no word has to be written into storage. By monitoring the Y_n lines, a convenient way of decoding an available address exists. Here exclusive OR circuitry is used which ensures that memory locations are filled successively when the need for "learning" exists. The quad latch is enabled before the write command is available to the CAM array. Thus the Y lines of unavailable memory locations are forced low ($Y_k = 0$).

A CLEAR command totally erases the memory contents and although it is simple to selectively erase words, for clarity it has not been discussed here.

TYPICAL APPLICATION

