

DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 8230 incorporates an INHIBIT input which, when low, allows the one-of-eight inputs selected by the address to appear on the f output and, in complement, on the $\bar{f}$ output. With the INHIBIT input high, the f output is unconditionally low and the $\bar{f}$ output is unconditionally high. The 8230 is a functional and pin-for-pin replacement for the 9312.

The 8231 is a variation of the 8230 that provides open collector output $\bar{f}$ for expansion of input terms. The 8232 is similar to the 8230 except in the effect of the INHIBIT input on the $\bar{f}$ output. With the INHIBIT low, the selected input appears at the f output and, in complement, on the $\bar{f}$ output. With the INHIBIT input high, both the f and the $\bar{f}$ output are unconditionally low.

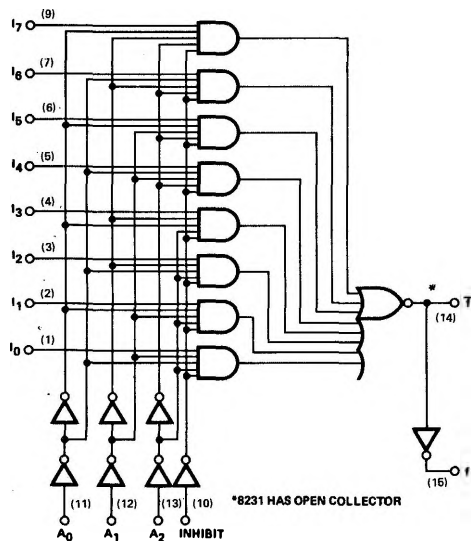
TRUTH TABLE

ADDRESS			DATA INPUTS									OUTPUT		
A ₂	A ₁	A ₀	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	INH	f	8230 8231 f	8232 f
0	0	0	x	x	x	x	x	x	1	1	0	1	0	0
0	0	1	x	x	x	x	x	1	x	x	0	1	0	0
0	1	0	x	x	x	x	1	x	x	x	0	1	0	0
0	1	1	x	x	x	x	1	x	x	x	0	1	0	0
1	0	0	0	x	x	1	x	x	x	x	0	1	0	0
1	0	1	x	x	1	x	x	x	x	x	0	1	0	0
1	1	0	x	1	x	x	x	x	x	x	0	1	0	0
1	1	1	0	x	1	x	x	x	x	x	0	1	0	0
1	1	1	1	x	x	x	x	x	x	x	0	1	0	0
0	0	0	x	x	x	x	x	x	x	0	0	0	1	1
0	0	1	x	x	x	x	x	0	x	x	0	0	1	1
0	0	1	1	x	x	x	x	0	x	x	0	0	1	1
1	0	0	0	x	x	0	x	x	x	x	0	0	1	1
1	0	1	x	0	x	x	x	x	x	x	0	0	1	1
1	1	0	0	x	0	x	x	x	x	x	0	0	1	1
1	1	1	0	x	0	x	x	x	x	x	0	0	1	1
1	1	1	1	0	x	x	x	x	x	x	0	0	1	1
x	x	x	x	x	x	x	x	x	x	x	1	0	1	0

x = don't care

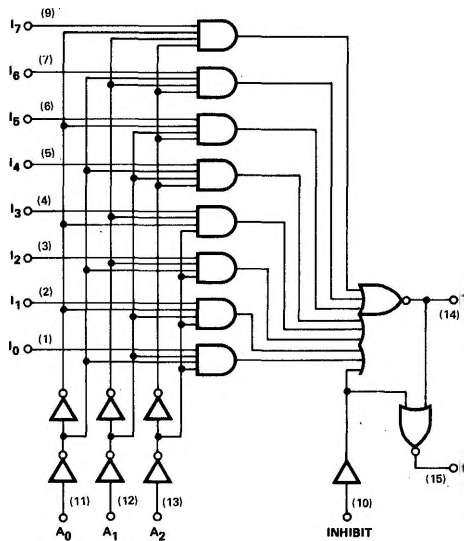
LOGIC DIAGRAMS

8230 AND 8231



V_{CC} = (16)
GND = (8)
() = Denotes Pin Numbers

8232



V_{CC} = (16)
GND = (8)
() = Denotes Pin Numbers

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	A ₁	A ₂	A ₃	INH	DATA INPUT I _{in}	OUTPUTS	
"1" Output Voltage, Output f	2.6	3.5		V	*	*	*	0.8V	2.0V	-800μA	6, 9
Output $\bar{f}$ (8230, 8232)	2.6	3.5		V	*	*	*	2.0V	*	-800μA	6, 9
"1" Output Leakage Current, Output $\bar{f}$ (8231)			150	μA	0.8V	2.0V	2.0V	2.0V	0.6V		11
"0" Output Voltage			0.4	V	0.8V	0.8V	0.8V	0.8V	0.8V	16mA	7, 9
"1" Input Current											
Inputs A _n , I _n			40	μA	4.5V	4.5V	4.5V		4.5V		
Input INH, 8230 & 8231			80	μA				4.5V			
Input INH, 8232			80	μA				4.5V			
"0" Input Current											
A _n , I _n , INH (8230 & 8231)	-0.1		-1.6	mA	0.4V	0.4V	0.4V		0.4V		
INH, (8232)	-0.1		-3.2	mA				0.4V			

T_A = 25°C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	A	A	A	INH	DATA INPUT I _{in}	OUTPUTS f $\bar{f}$	
Propagation Delay											
A _n to $\bar{f}$ (8230, 8232)		19	30	ns							8
A _n to $\bar{f}$ (8231)		17	30	ns							8
I _n to $\bar{f}$ (8230, 8232)		11	20	ns							8
$\bar{f}$ to f		10	15	ns							8
I _n to $\bar{f}$ (8231)		13	24	ns							8
INH to $\bar{f}$ (8230, 8231)		18	30	ns							8
INH to f or $\bar{f}$ (8232)		11	20	ns							8
Power Consumption/Supply Current											
8230, 8231		184/ 35	250/ 47.7	mW/mA	4.5V	4.5V	4.5V	4.5V	0V		10
8232		173/ 33	262/ 50.0	mW/mA	4.5V	4.5V	4.5V	4.5V	0V		10
Output Short Circuit Current											
Output f	-20		-70	mA	0V	0V	0V	0V	4.5V	0V	10, 12
Output $\bar{f}$ (8230, 8232)	-20		-70	mA	0V	0V	0V	0V	0V	0V	10, 12
Input Voltage Rating	5.5			V	10mA	10mA	10mA	10mA	10mA		

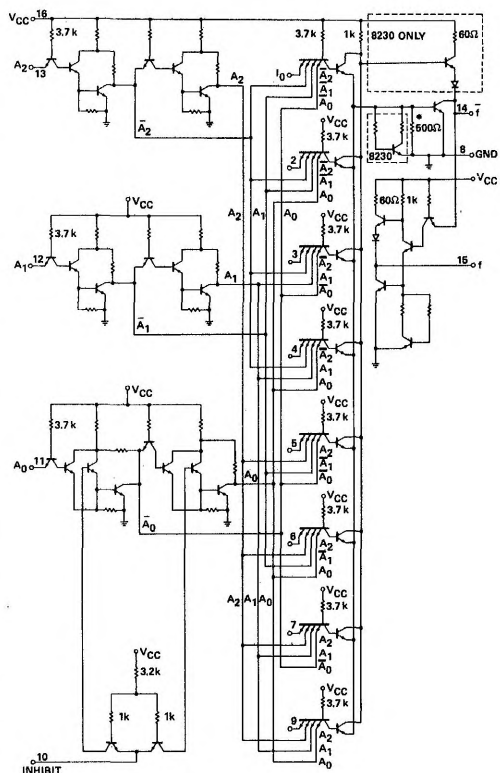
*See Truth Table for Logical Conditions

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with groundpin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figures.
9. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
10. All I_n data inputs are at 0V. V_{CC} = 5.25V.
11. Connect an external 1k resistor from V_{CC} to the output terminal for this test.
12. Not more than one output should be shorted at a time.

SCHEMATIC DIAGRAMS

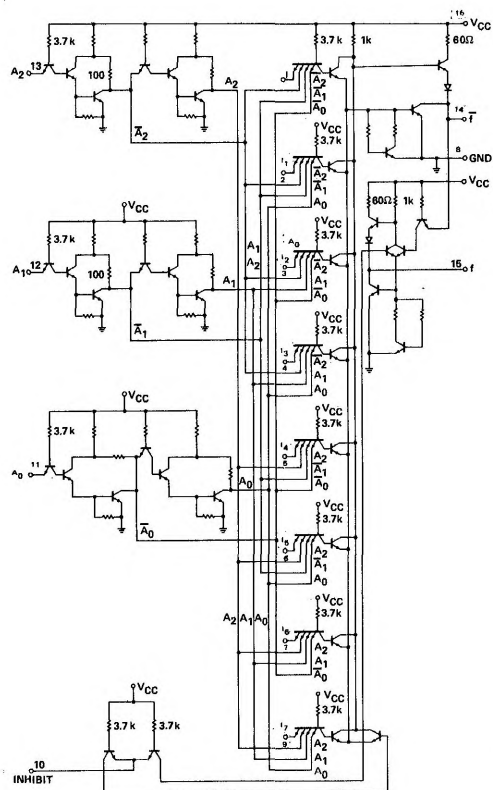
8230 AND 8231



*500 Resistor on 8231 only.

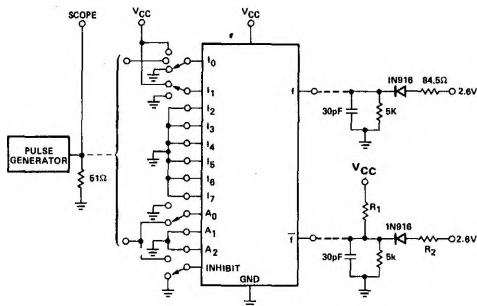
Note: All inputs have diode clamping. All outputs have isolation diodes.

8232



Note: All inputs have diode clamping. All outputs have isolation diodes.

AC TEST FIGURE AND WAVEFORMS

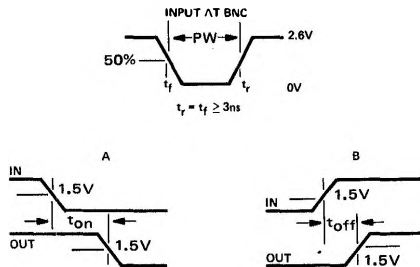


	8320/32	8231
R_1	∞	360Ω
R_2	84.5Ω	440Ω

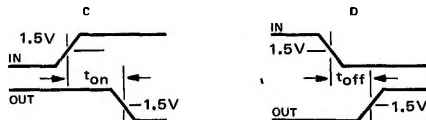
NOTES:

1. $5K$, $30pF$ load includes test jigs and scope impedance.
2. Scope terminals to be $\leq 1\frac{1}{2}''$ from package pins.
3. See truth table for logical conditions.

NON-INVERTING PATHS



INVERTING PATHS



AC TEST CONDITIONS

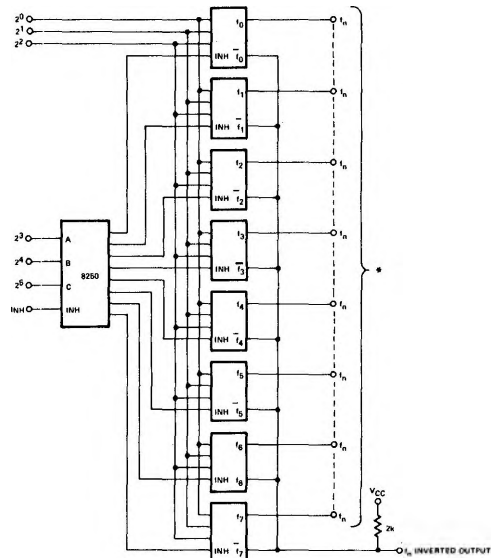
STEP NO.	TYPE/S	DELAY FROM-TO	INPUTS				WAVE-FORM TYPE
			I_0	I_1	A_0	INH	
1	ALL	A_0 to $\bar{f}$	0 V	V_{CC}	P.G.	0 V	C, D
2	ALL	I_0 to $\bar{f}$	P.G.	0 V	0 V	0 V	C, D
3	ALL	$\bar{f}$ to f^*	P.G.	0 V	0 V	0 V	C, D
4	8230 8231	INH to $\bar{f}$	V_{CC}	0 V	0 V	P.G.	A, B
5	8232	INH to $\bar{f}$	0 V	0 V	0 V	P.G.	C, D
6	8232	INH to f	V_{CC}	0 V	0 V	P.G.	C, D

NOTE: 1. P. G. = Pulse Generator

*Both f and $\bar{f}$ are simultaneously loaded.

TYPICAL APPLICATIONS

EXPANSION OF 8231 TO MULTIPLEXER 64 LINES



$$*f_n = f_0 + f_1 + f_2 \dots f_7$$

True Output

All Outputs may be tied together to drive $8 \times 16mA$ (eight $1.6mA$ F.O.) or each Output may drive separately ten $1.6mA$ F.O.

Note:

Each 8231 has 8 data inputs which are not shown.