# intel®

Silicon Gate MOS **8253**

PROGRAMMABLE INTERVAL TIMER

- **3 Independent 16-Bit Counters**
- **DC to 3 MHz**
- **Programmable Counter Modes**

- **Count Binary or BCD**
- **Single +5V Supply**
- **24 Pin Dual-in-line Package**

The 8253 is a programmable counter/timer chip designed for use as an 8080 (or 8008) peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as three independent 16-bit counters, each with a count rate from 0Hz to 3MHz. All modes of operation are software programmable by the 8080.

PIN CONFIGURATION
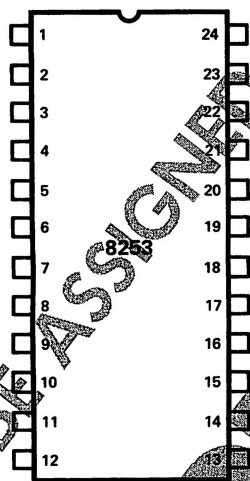
BLOCK DIAGRAM
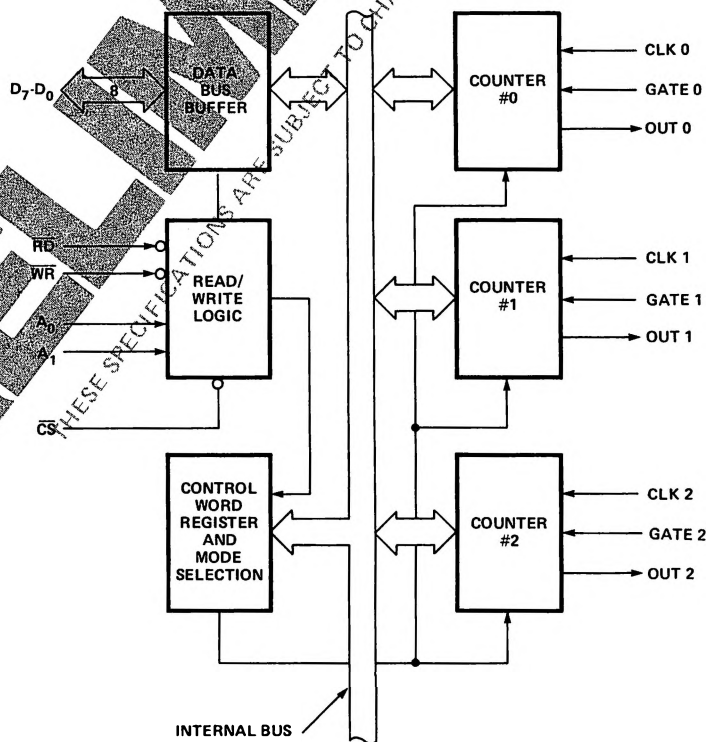
8253 PRELIMINARY FUNCTIONAL DESCRIPTION

In Microcomputer-based systems the most common interface is to a mechanical device such as a printer head or stepper motor. All such devices have inherent delays that must be accounted for if accurate and reliable performance is to be achieved. The systems software allows for such delays by programmed timing loops. This type of programming requires significant overhead and maintenance of multiple loops gets extremely complicated.

The 8253 Programmable Interval Timer is a single chip solution to system timing problems. In essence, it is a group of three 16-bit counters that are independent in nature but driven commonly as I/O peripheral ports. Instead of setting up timing loops in the system software, the programmer configures the 8253 to match his requirements. The programmer initializes one of the three counters of the 8253 with the quantity and mode desired then, upon command, the 8253 will count out the delay and interrupt the microcomputer when it has finished its task. It is easy to see that the software overhead is minimal and that multiple delays can be easily maintained by assigned interrupt levels to different counters. Other functions that are non-delay in nature and require counters can also be implemented with the 8253.

- Programmable Baud Rate Generator
- Event Counter
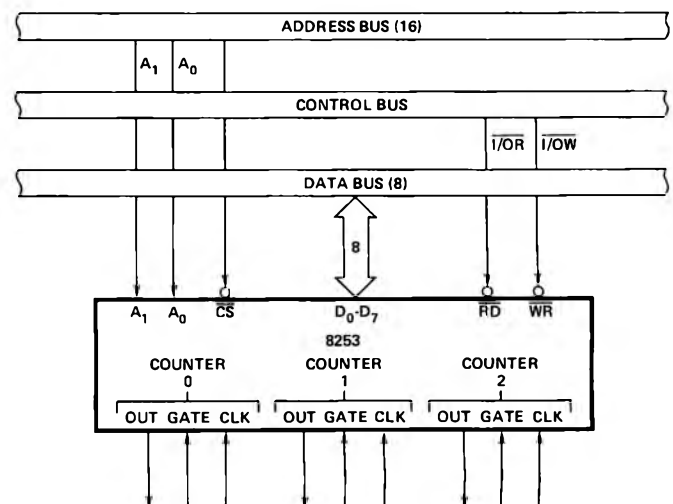- Binary Rate Multiplier
- Real Time Clock

System Interface

The 8253 is a component of the MCS-80 system and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of I/O ports; three are counters and the fourth is a control register for programming. The OUT lines of each counter would normally be tied to the interrupt request inputs of the 8259.

The 8253 represents a significant improvement for solving one of the most common problems in system design and reducing software overhead.
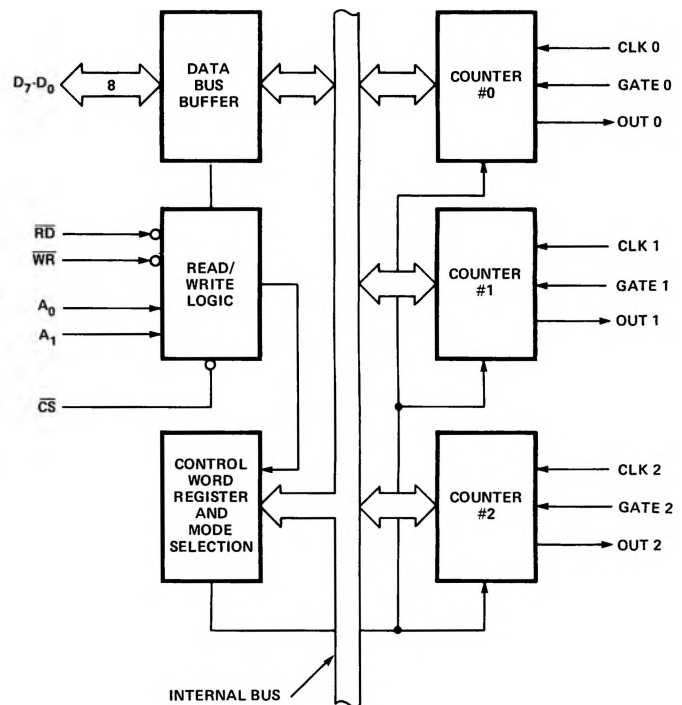
8253 Block Diagram.

8253 System Interface.