DESCRIPTION

The 8270 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

The internal design uses level sensitive binaries which respond to the negative-going clock transition. A buffer clock driver has been included to minimize input clock loading.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control.

The truth table for the control modes is shown below.

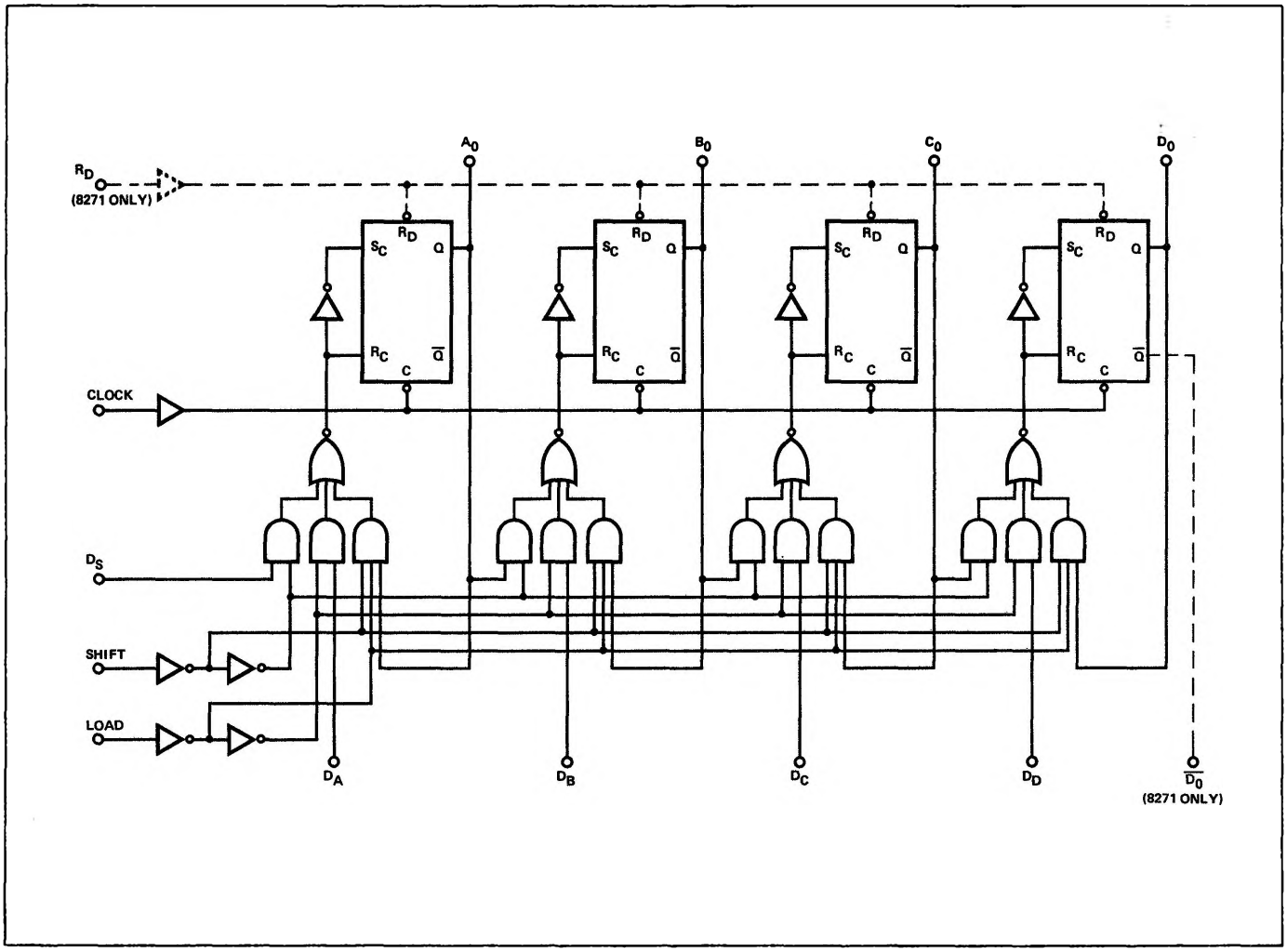
For applications not requiring the hold mode, the load input may be tied high and the shift input used as the mode control.

The 8271 provides a direct reset (R_D), and a $\overline{D_{out}}$ line in addition to the available outputs of the 8270 element. The fan-out specification for this output is the same as the true outputs of the 8270 element.

TRUTH TABLE

CONTROL STATE	LOAD	SHIFT
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	LOAD	SHIFT	DATA INPUT	CLOCK	RESET 8271	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	2.0V	0.8V	2.0V	Pulse	2.0V	-800μA	6
"0" Output Voltage			0.4	V	2.0V	0.8V	0.8V	Pulse	2.0V	11.2mA	7
"0" Input Current											
Load	-0.1		-1.2	mA	0.4V						
Shift	-0.1		-1.2	mA		0.4V					
Data Input	-0.1		-1.2	mA			0.4V				
Clock	-0.1		-1.2	mA				0.4V			
Reset (8271 only)	-0.1		-1.2	mA					0V		
"1" Input Current											
Load			40	μA	4.5V						
Shift			40	μA		4.5V					
Data Input			40	μA			4.5V				
Clock			40	μA				4.5V			
Reset (8271 only)			40	μA					4.5V		
Input Voltage Rating											
(All Inputs)	5.5			V	10mA	10mA	10mA	10mA	10mA		

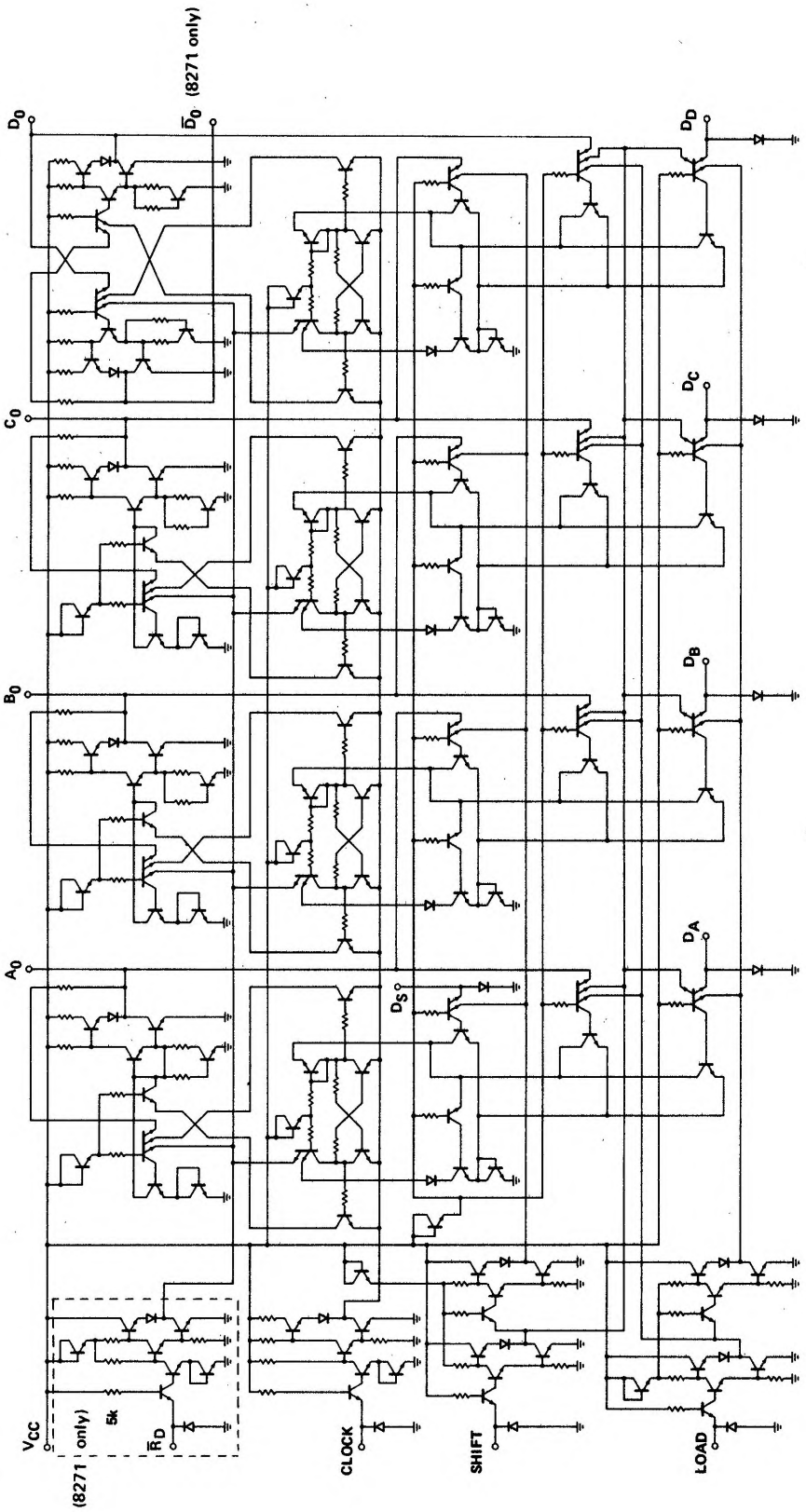
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS						NOTES
	MIN.	TYP.	MAX.	UNITS	LOAD	SHIFT	DATA INPUT	CLOCK	RESET 8271	OUTPUTS	
Power/Current Consumption											
8270 Only		168/32	247/47	mW/mA							10
8271 Only		271/52	344/65	mW/mA							10
Turn-On Delay											
All Binaries		25	40	ns							8
Turn-Off Delay											
All Binaries		25	40	ns							8
Clock "1" Interval	20			ns				2.0V			
Transfer Rate	15	22		MHz							
Shift Load Set-Up Time		20	30	ns							
Data Set-Up Time		7	15	ns							

NOTES:

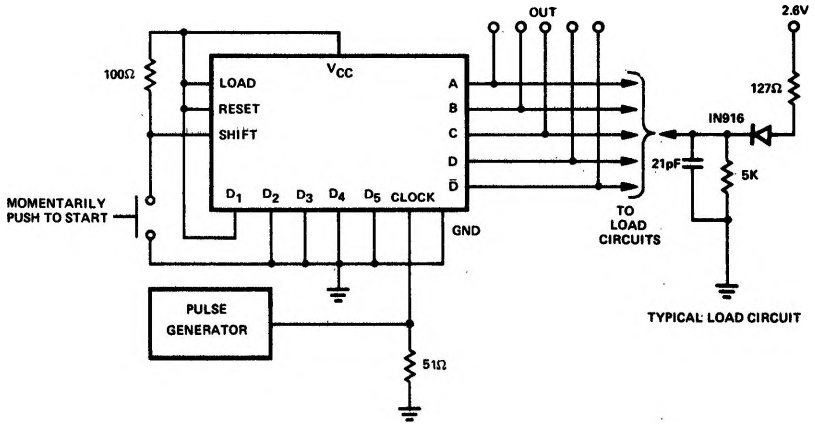
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Rating should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. V_{CC} = 5.25 volts.

SCHEMATIC DIAGRAM



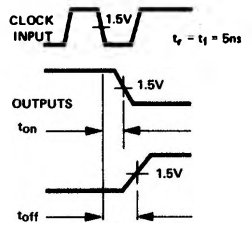
AC TEST FIGURES AND WAVEFORMS

TURN ON/OFF AND TRANSFER RATE



NOTES:

1. t_{on}/ t_{off}



2. Transfer rate & min clock "1" level: check that binary outputs are changing.

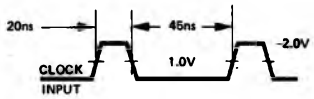
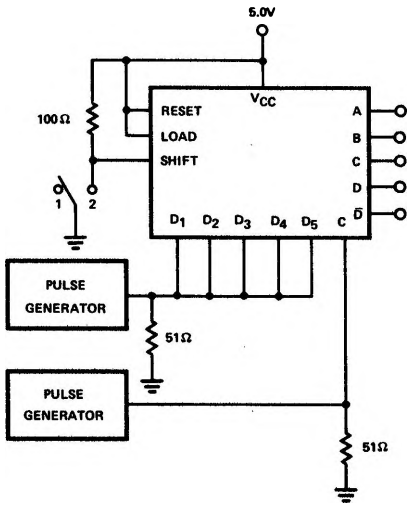
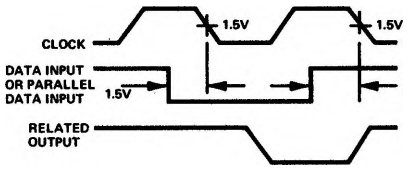


FIGURE 1

DATA SET-UP TIME



Load see Figure 1 above.



NOTES:

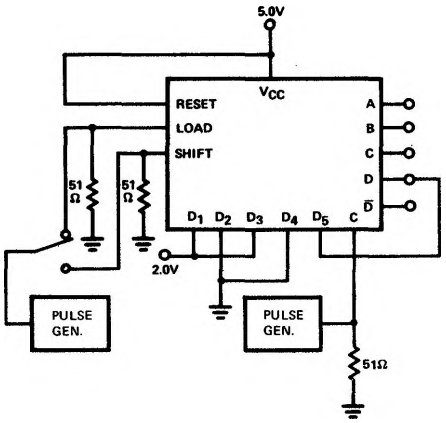
1. Switch in position 1 to test serial data input.
2. Switch in position 2 to test parallel data input.

Adjust data input or parallel input delays to test condition and verify output operation.

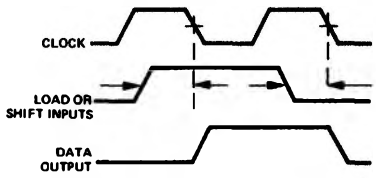
FIGURE 2

AC TEST FIGURES AND WAVEFORMS (Cont'd)

SHIFT/LOAD SET-UP TIME



Load see Figure 1 Page 106.



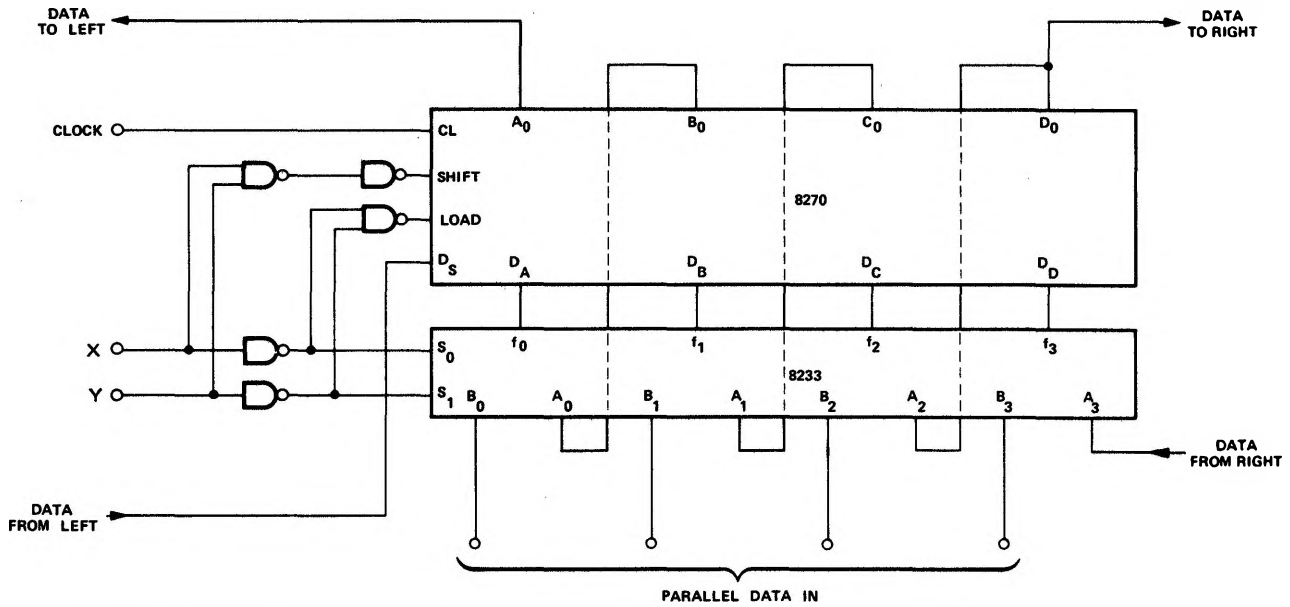
NOTE:
Determine proper Q output state using switch position and load or shift input state before clocking transition.

FIGURE 3

NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent, f = 1 MHz, V_{AC} = mV rms.
3. All diodes are 1N916.

TYPICAL APPLICATIONS

SHIFT-RIGHT/SHIFT-LEFT/PARALLEL ENTRY SHIFT REGISTER



X	Y	Function
0	0	Hold
0	1	Shift Left
1	0	Parallel Load
1	1	Shift Right

Package Count: 1-8270
1-8233
½-8H90
½-8H80