# 8-BIT SHIFT REGISTER | 8276

**PRODUCT AVAILABLE IN 0°C TO 75°C TEMP RANGE ONLY.**

**DIGITAL 8000 SERIES TTL/MSI**

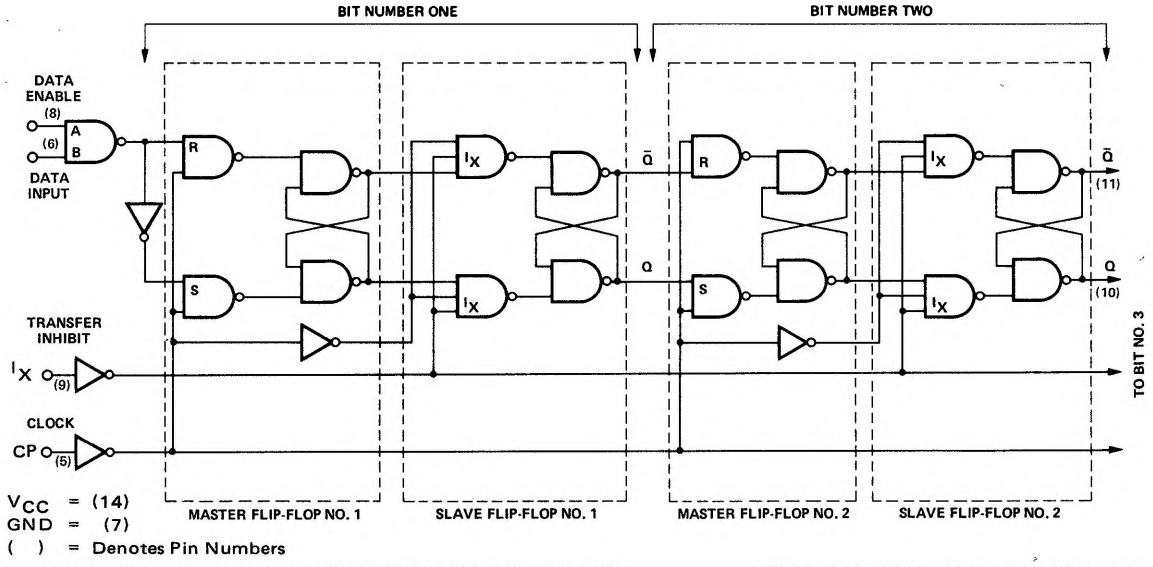
## DESCRIPTION

The 8276 is a serial-in, serial-out 8-Bit Shift Register composed of eight R-S master slave flip-flops. This shift register has input gating and an internal clock driver. In addition, a data transfer inhibit input is provided.

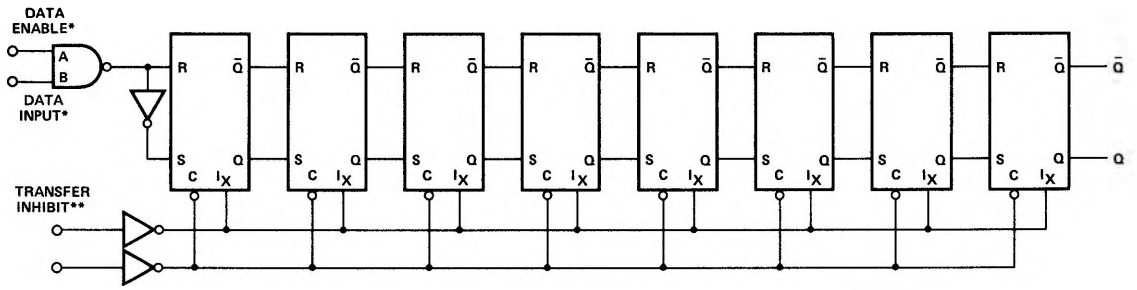
Data Input and Data Enable are gated through inputs A and B. An internal inverter provides the complimentary inputs to the first bit of the shift register. All inputs are fully buffered. Complementary Q and $\overline{Q}$ outputs are provided.

The internal clock driver/inverter causes the 8276 to shift data to the output on the positive edge of the input clock pulse, making the shift register compatible with the 8825 J-K Binary and the 8828 Dual D type Binary. The register is inhibited from shifting data when the Transfer Inhibit line is high. The inhibit function is achieved by preventing data transfer from master to slave sections of the register elements when the inhibit line is used.

## LOGIC DIAGRAMS AND TRUTH TABLES




$V_{CC}$ = (14)
GND = (7)
( ) = Denotes Pin Numbers




| $t_n$ | | $t_{n+8}$ |
|---|---|---|
| A (Data Enable) | B (Data Input) | Q |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

*NOTE: These functions are interchangeable.
**NOTE: Transfer Inhibit prevents transfer of data from master to slave.

NOTES:
$t_n$ = Bit time before clock pulse.
$t_{n+8}$ = Bit time after 8 clock pulses.

## ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

| CHARACTERISTICS | LIMITS | | | | TEST CONDITIONS | | | | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | UNITS | DATA INPUTS | CLOCK | TRANS. INHIBIT | OUTPUTS | |
| "1" Output Voltage Q | 2.6 | | | V | 2.0V | | 0.8V | -800μA | 6, 10 |
| "1" Output Voltage $\overline{Q}$ | 2.6 | | | V | 0.8V | | 0.8V | -800μA | 6, 10 |
| "0" Output Voltage Q | | | 0.4 | V | 0.8V | | 0.8V | 16mA | 7, 10 |
| "0" Output Voltage $\overline{Q}$ | | | 0.4 | V | 2.0V | | 0.8V | 16mA | 7, 10 |
| "0" Input Current | | | | | | | | | |
| Data Input | -0.1 | | -1.6 | mA | 0.4V | | | | |
| Clock Input | -0.1 | | -1.6 | mA | | 0.4V | | | |
| Inhibit Input | -0.1 | | -1.6 | mA | | | 0.4V | | |
| "1" Input Current | | | | | | | | | |
| Data Inputs | | | 40 | μA | 4.5V | | | | |
| Clock Input | | | 40 | μA | | 4.5V | | | |
| Inhibit Input | | | 40 | μA | | | 4.5V | | |
| Input Voltage Rating | 5.5 | | | V | 10mA | 10mA | 10mA | | |

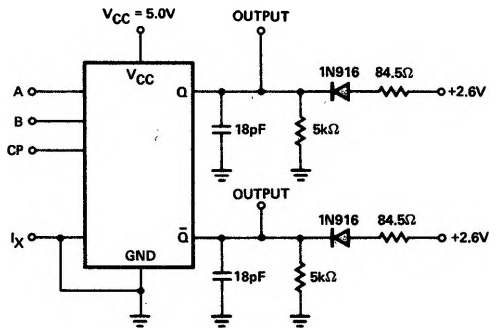
### $T_A = 25°C$ and $V_{CC} = 5.0V$

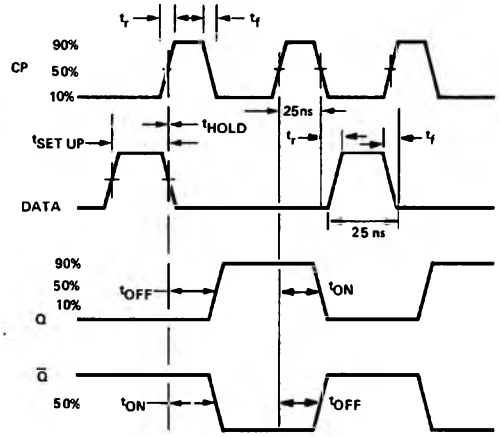
| CHARACTERISTICS | LIMITS | | | | TEST CONDITIONS | | | | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | UNITS | DATA INPUTS | CLOCK | TRANS. INHIBIT | OUTPUTS | |
| Power/Current Consumption | | 205/39 | 340/65 | mW/mA | | | | | 11 |
| Transfer Rate | 15 | 20 | | MHz | | | | | |
| Turn-on Delay | | | | | | | | | |
| (Clock to Output) | | 22 | 33 | ns | | | | | 8 |
| Turn-off Delay | | | | | | | | | |
| (Clock to Output) | | 22 | 33 | ns | | | | | 8 |
| Clock Pulse Width | 25 | | | ns | | | | | |
| Set Up Time (Logical) | | | | | | | | | |
| "0" at A or B Input | 25 | | | ns | | | | | |
| Set Up Time (Logical) | | | | | | | | | |
| "1" at A or B Input | 25 | | | ns | | | | | |
| Output Short Circuit Current | -18 | | -55 | mA | | | | 0V | |

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to $V_{CC}$.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Clock input is driven by a 1kHz square wave for at least 8 cycles prior to measurements.
11. $V_{CC} = 5.25V$.

## AC TEST FIGURE AND WAVEFORMS



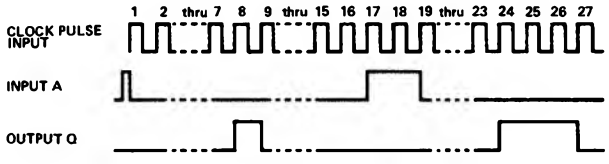




NOTES:
1. Unused input connected to 2.6V
2. Input pulse characteristics:
3. Setup time = 25ns
   Hold time = 0ns

CLOCK:
Amplitude = 3.0V
$t_r = t_f$ = 5ns max
PRR = 15 MHz, Pulse width = 25ns at 50% points

INPUT:
Amplitude = 3.0V
$t_r = t_f$ = 5ns max
PRR = 7.5 MHz
Pulse width = 25ns at 50% points

### TYPICAL INPUT/OUTPUT WAVEFORMS




NOTE: Input B is connected to 2.6V. Transfer Inhibit Connected to 0V