

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S126 and 82S129 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, F or N, and for the military temperature range (-55°C to +125°C) specify S82S126/129, F only.

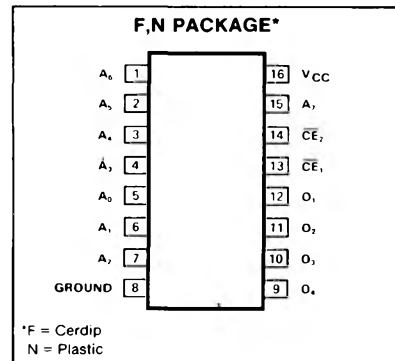
FEATURES

- **Address access time:**
N82S126/129: 50ns max
S82S126/129: 70ns max
- **Power dissipation:** 0.5mW/bit typ
- **Input loading:**
N82S126/129: -100 μ A max
S82S126/129: -150 μ A max
- **On-chip address decoding**
- **Output options:**
82S126: Open collector
82S129: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

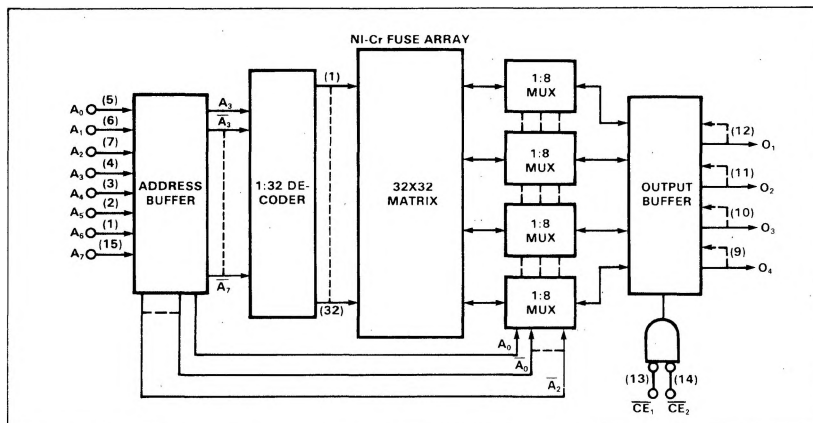
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
V _{OH}	Output voltage		Vdc
VOH	High (82S126)	+5.5	
VO	Off-state (82S129)	+5.5	
TA	Temperature range		°C
	Operating		
	N82S126/129	0 to +75	
	S82S126/129	-55 to +125	
T _{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N82S126/129: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S126/129: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TEST CONDITIONS ¹	N82S126/129			S82S126/129			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V_{IL} V_{IH} V_{IC}	Input voltage Low High Clamp $I_{IN} = -18\text{mA}$	2.0	-0.8	.85 -1.2	2.0	-0.8	.80 -1.2	V
V_{OL} V_{OH}	Output voltage Low High (82S129) $I_{OUT} = 16\text{mA}$ $\overline{CE}_1 = \overline{CE}_2 = \text{Low}$, $I_{OUT} = -2.0\text{mA}$, High stored	2.4		0.45	2.4		0.5	V
I_{IL} I_{IH}	Input current Low High $V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$			-100 40			-150 50	μA
I_{OLK} $I_{O(OFF)}$	Output current Leakage (82S126) Hi-Z state (82S129) $\overline{CE}_1$ or $\overline{CE}_2 = \text{High}$, $V_{OUT} = 5.5\text{V}$ $\overline{CE}_1$ or $\overline{CE}_2 = \text{High}$, $V_{OUT} = 5.5\text{V}$ $\overline{CE}_1$ or $\overline{CE}_2 = \text{High}$, $V_{OUT} = 0.5\text{V}$			40 40 -40			60 60 -60	μA μA
I_{OS}	Short circuit (82S129) $V_{OUT} = 0\text{V}$	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current		105	120		105	125	mA
C_{IN} C_{OUT}	Capacitance Input Output $V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		5 8			5 8		pF

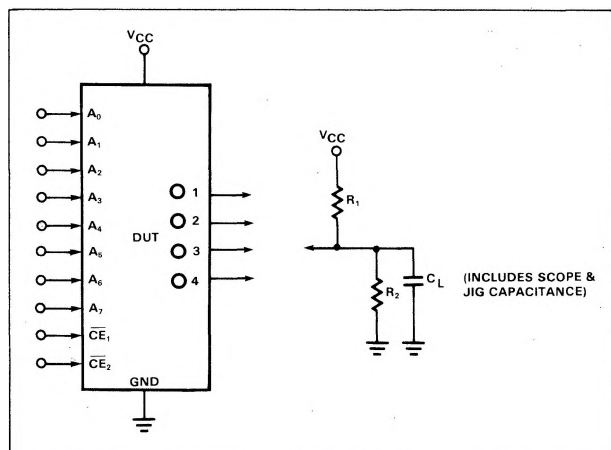
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$
 N82S126/129: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S126/129: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N82S126/129			S82S126/129			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
T_{AA} T_{CE}	Access time Output Output	Address Chip enable		35 15	50 25		35 15	70 35	ns
T_{CD}	Disable time Output	Chip disable		15	25		15	35	ns

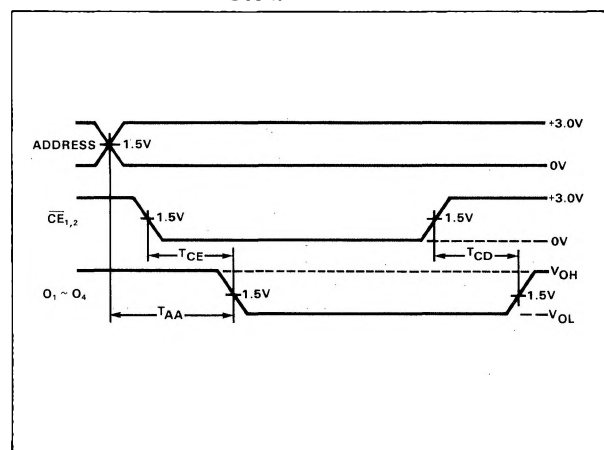
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $T_A = +25^{\circ}\text{C}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CCP} Power supply voltage To program ¹	$I_{CCP} = 375 \pm 75\text{mA}$, Transient or steady state	8.5	8.75	9.0	V
V_{CCH} Verify limit Upper		5.3	5.5	5.7	V
V_{CCL} Lower		4.3	4.5	4.7	
V_S Verify threshold ²		1.4	1.5	1.6	V
I_{CCP} Programming supply current	$V_{CCP} = +8.75 \pm .25\text{V}$	300		450	mA
V_{IH} Input voltage High		2.4		5.5	V
V_{IL} Low		0	0.4	0.8	
I_{IH} Input current High	$V_{IH} = +5.5\text{V}$			50	μA
I_{IL} Low	$V_{IL} = +0.4\text{V}$			-500	
V_{OUT} Output programming voltage ³	$I_{OUT} = 200 \pm 20\text{mA}$, Transient or steady state	16.0	17.0	18.0	V
I_{OUT} Output programming current	$V_{OUT} = +17 \pm 1\text{V}$	180	200	220	mA
T_R Output pulse rise time		10		50	μs
t_p $\overline{\text{CE}}$ programming pulse width		0.3	0.4	0.5	ms
t_D Pulse sequence delay		10			μs
T_{PR} Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PSI} Initial programming pause	$V_{CC} = 0\text{V}$	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$ Programming duty cycle ⁴				50	%
F_L Fusing attempts per link				2	cycle

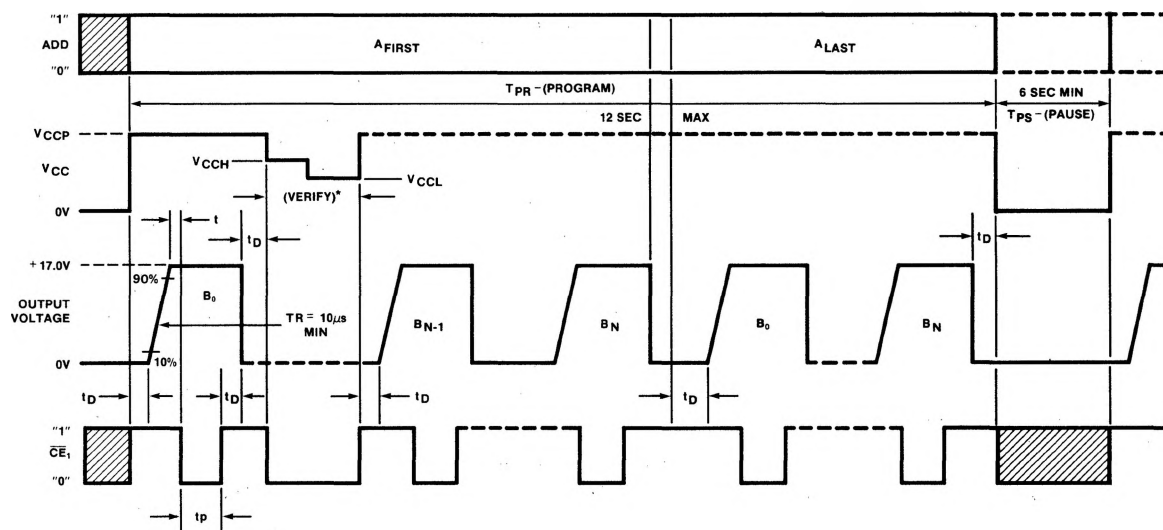
NOTES

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10\text{k}\Omega$ resistor to V_{CC} . Apply $\overline{\text{CE}}_1 = \text{High}$, $\overline{\text{CE}}_2 = \text{Low}$.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$.
3. After $10\mu\text{s}$ delay, apply $V_{OUT} = +17 \pm 1\text{V}$ to the output to be programmed. Program one output at the time.
4. After $10\mu\text{s}$ delay, pulse the $\overline{\text{CE}}_1$ input to logic low for 0.3 to 0.5ms.
5. After $10\mu\text{s}$ delay, remove $+17\text{V}$ from the programmed output.
6. To verify programming, after $10\mu\text{s}$ delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2\text{V}$, and apply a logic low level to the $\overline{\text{CE}}$ input. The programmed output should remain in the high state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2\text{V}$, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$, and repeat steps 3 through 6 to program other bits at the same address.
8. After $10\mu\text{s}$ delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.