DESCRIPTION

The 82S16/116 and 82S17/117 are read/write memory arrays which feature either open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors which reduce input loading to 25μA for a high level, and −100μA for a low level.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write-Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

All devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82S16/116/17/117, F or N. The 82S16 and 82S17 are also available in the military temperature range (−55°C to +125°C) and are specified as S82S16/17.

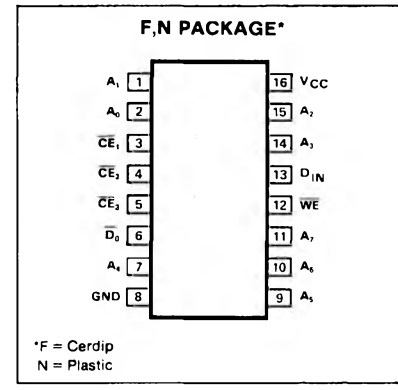
FEATURES

- **Address access time:**
  82S116/117: 40ns max
- **Write cycle time:**
  82S116/117: 25ns max
- **Power dissipation: 1.5mW/bit typ**
- **Input loading:**
  N82S116/117: −100μA
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Output option:**
  82S16/116: Tri-state
  82S17/117: Open collector
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



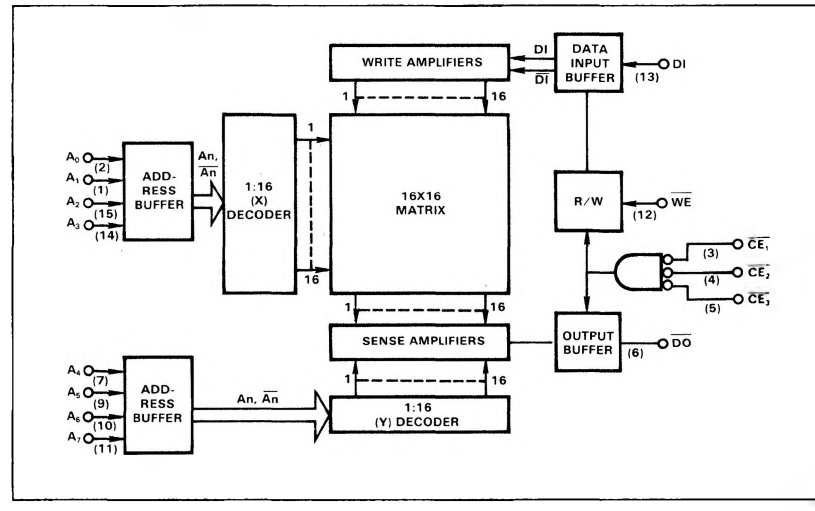
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S16/116	82S17/117
Read	0	1	X	Stored $\overline{data}$	Stored $\overline{data}$
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	0
Diasabled	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage	+5.5	Vdc
V_{OUT}	High (82S17)		
V_O	Off-state (82S16)		
	Temperature range		°C
T_A	Operating		
	S82S16/17	-55 to + 125	
	N82S16/17, N82S116/117	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S116/117, N82S16/17: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S16/17: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS	N82S16/17/116/117			S82S16/17			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage[2]								V
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage[2]	V_{CC}= Min							V
V_{OH}	High (82S16/116)[4]	I_{OH} = -3.2mA	2.6			2.4			
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45		0.35	0.5	
	Input current[3]	V_{CC} = Max							mA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-250	
	Output current								
I_{OLK}	Leakage (82S17/117)[6]	V_{OUT} = 5.5V		1	40		1	40	μA
$I_{O(OFF)}$	Hi-Z state (82S16/116)[6]	V_{OUT} = 5.5V		1	40		1	50	μA
		V_{OUT} = 0.45V		-1	-40		-1	-50	
I_{OS}	Short-circuit (82S16/116)[7]	V_{CC} = Max, V_O = 0V	-20		-70	-20		-70	μA
I_{CC}	V_{CC} supply current	V_{CC} = Max		80	115		80	120	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

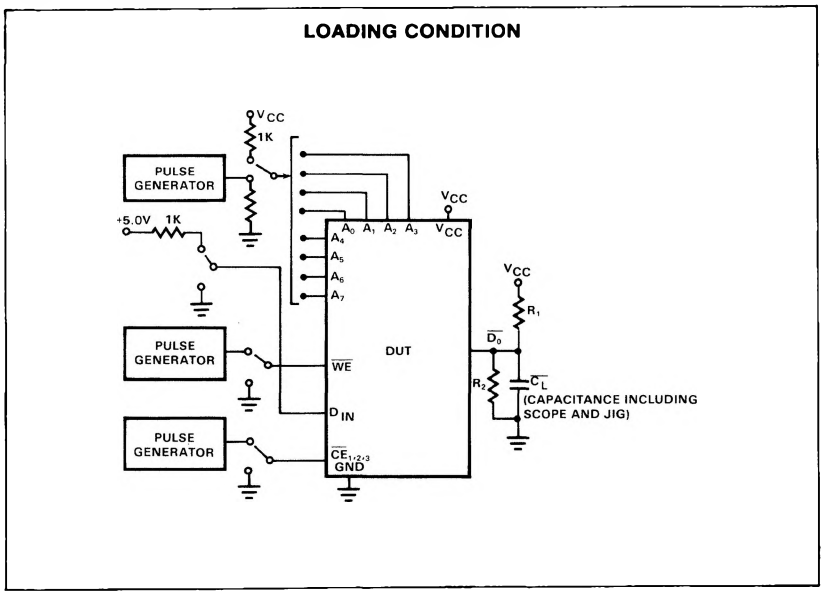
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S116/117, N82S16/17: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S16/17: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S16/17			N82S116/117			S82S16/17			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time												ns
T_{AA}	Address				40	50		30	40		40	70	
T_{CE}	Chip enable				30	40		15	25		30	40	
T_{CD}	Disable time	Output	Chip enable		30	40		15	25		30	40	ns
T_{WD}	Valid time	Output	Write enable		30	40		30	40		30	55	ns
	Setup and hold time												ns
T_{WSA}	Setup time	Write enable	Address	20	5		0	-5		20	5		
T_{WHA}	Hold time			5	0		0	-5		10	0		
T_{WSD}	Setup time	Write enable	Data in	40	30		25	15		50	40		
T_{WHD}	Hold time			5	0		0	-5		10	0		
T_{WSC}	Setup time	Write enable	$\overline{CE}$	10	0		0	-5		10	0		
T_{WHC}	Hold time			5	0		0	-5		10	0		
	Pulse width												ns
T_{WP}	Write enable[8]			30	15		25	15		40	20		

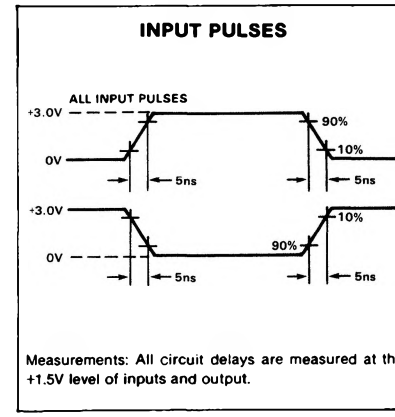
NOTES

1. All typical values are at $V_{CC} = 5V$, T_A +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at the time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.

TEST LOAD CIRCUIT



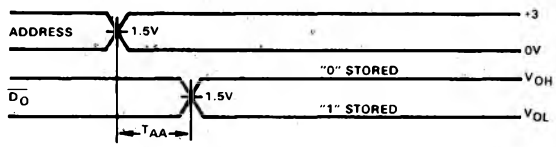
VOLTAGE WAVEFORM



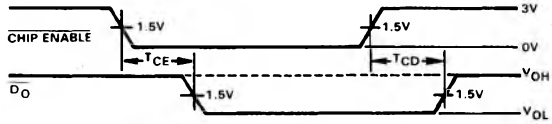
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS

READ CYCLE

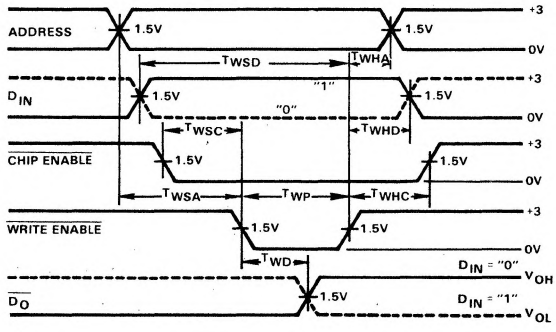


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.