

DESCRIPTION

The 82S208 and 82S210 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

The address inputs have a latch feature controlled by a latch control pin ($\overline{L}$). In the Transparent mode, the $\overline{L}$ pin is held high and the read or write location is accessed directly from the address inputs. In the Latched mode, a negative transition on the $\overline{L}$ line causes the present address state to be

held in the address latches, independent of any other control signals. A positive pulse on the $\overline{L}$ line will cause a new address state to be strobed into the latches.

FEATURES

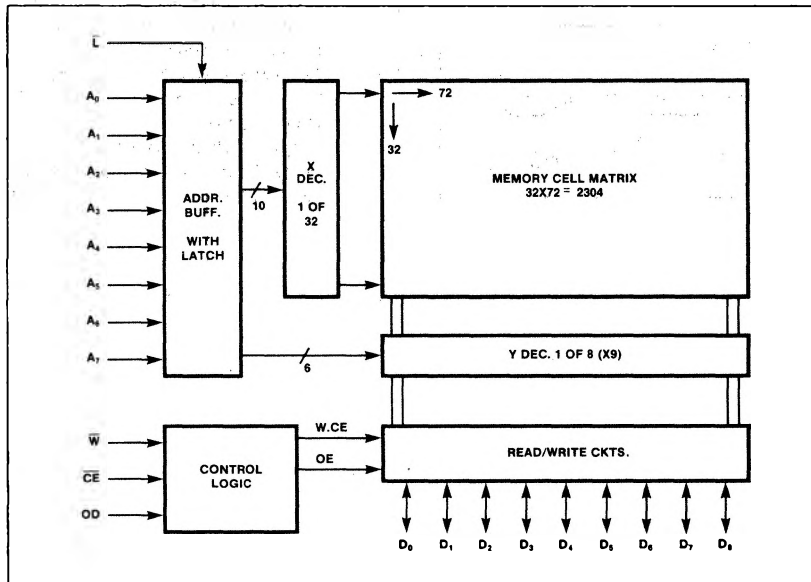
- Access time:
Address: 60ns max
Strobe: 70ns max
- On-chip address latches
- Tri-state outputs
- Schottky clamped TTL

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	OD	$\overline{L}$	D _N IN/OUT
Disable output	X	X	1	X	High Z
Disable R/W	X	1	X	X	High Z
Write	0	0	1	X	Data in
Read	1	0	0	X	Data out
Transparent address	X	X	X	1	—
Hold address	X	X	X	0	—

X = Don't care

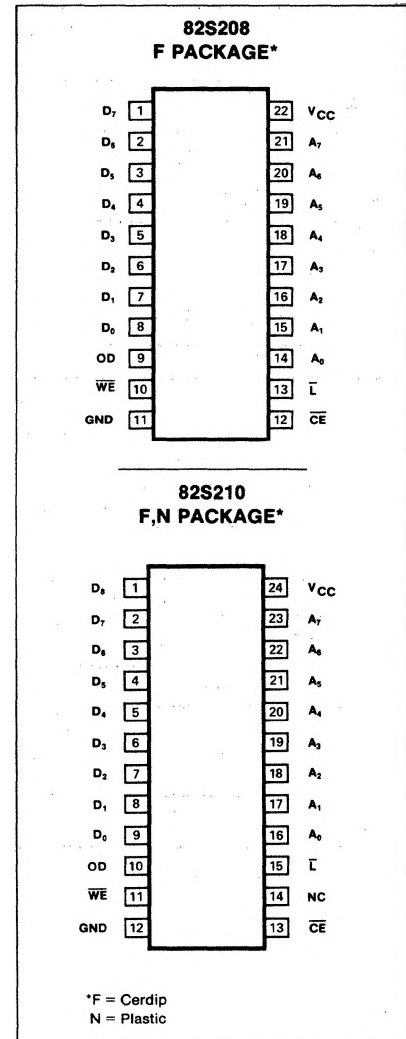
BLOCK DIAGRAM



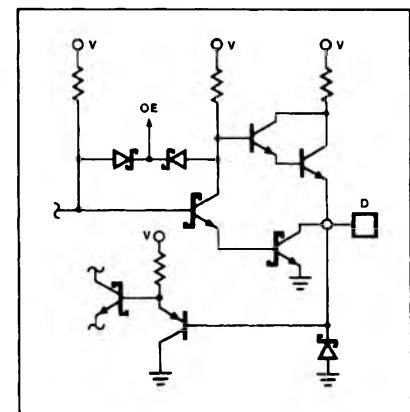
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Off-state output voltage	+5.5	Vdc
Temperature range		°C
T _A Operating	0 to +75	
T _{STG} Storage	-65 to +150	

PIN CONFIGURATION



TYPICAL I/O STRUCTURE



OBJECTIVE SPECIFICATION

82S208-F • 82S210-F,N

DC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A + 75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}^1$

PARAMETER	TEST CONDITIONS	LIMITS ²			UNIT
		Min	Typ ³	Max	
V_{IL} V_{IH} V_{IC}	Input voltage Low High Clamp ⁴	2.0	-0.8	.85	V
				-1.2	
V_{OL} V_{OH}	Output voltage Low High	2.4	3.3	0.5	V
I_{IL} I_{IH}	Input current Low High			-100 25	μA
$I_{O(OFF)}$ I_{OS}	Output current Hi-Z state Short circuit ^{4,5}	-20		40 -100 -70	μA mA
I_{CC}	Supply current		135	185	mA
C_{IN} C_{OUT}	Capacitance Input Output		5 8		pF

AC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
T_{AA} T_{AL}	Access time Address Strobe	Output Output			60 70	ns
T_{OE} T_{CE}	Enable time Output Output	Output Output			35 35	ns
T_{OD} T_{CD}	Disable time Output Output	Output Output			35	ns
T_{WL} T_{W}	Pulse width Strobe Write		20 40			ns
T_{SL} T_{HL} T_{SSA}	Setup and hold time Setup time Hold time Setup time (strobe)	Latch Address Latch	5 10 0			ns
T_{SC} T_{HC}	Setup time Hold time	Write Chip enable	5			
T_{SD} T_{HD}	Setup time Hold time	Write Data	35 10			
T_{SA} T_{HA}	Setup time Hold time	Write Address	10			
T_{SLW} T_{HLW}	Setup time Hold time	Write Latch	15 10			
T_{S01} T_{S02}	Setup time (from disabled state) Setup time (from enabled state)	Chip enable Data in	5 35			
T_{HO}	Hold time	OD Chip enable	5			

NOTES on following page.

OBJECTIVE SPECIFICATION

82S208-F • 82S210-F,N

NOTES

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.

TIMING DIAGRAMS

