DESCRIPTION

The 82S214 and 82S215 include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

Both 82S214 and 82S215 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S214/215, F or N, and for the military temperature range (-55°C to +125°C) specify S82S214/215, F.

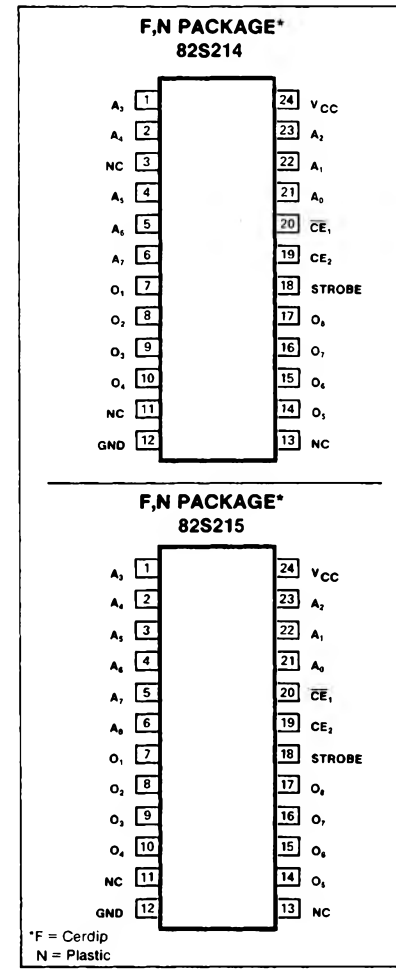
FEATURES

- **Address access time:**
  N82S214/215: 60ns max
  S82S214/215: 90ns max
- **Power dissipation: 165μW/bit typ**
- **Input loading:**
  N82S214/215: -100μA max
  S82S214/215: -150μA max
- **On-chip data output registers**
- **On-chip storage latches**
- **Schottky clamped**
- **Fully compatible with Signetics 82S114/115 PROMs**
- **Fully TTL compatible**

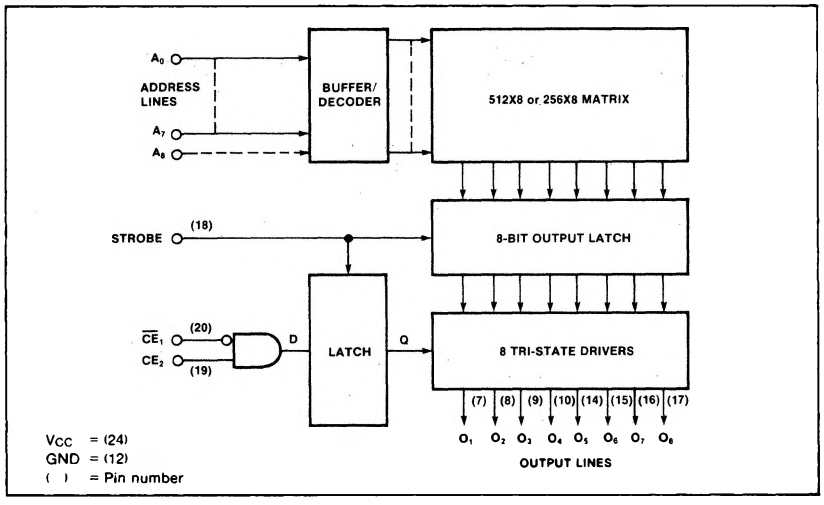
APPLICATIONS

- **Microprogramming**
- **Hardwire algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating		
	N82S214/215	0 to +75	
	S82S214/215	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S214/215: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S214/215: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S214/215			S82S214/215			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA			0.5			0.5	
V_{OH}	High	CE_1 = Low, CE_2 = High, I_{OUT} = -2mA, High stored	2.7	3.3		2.4	3.3		
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			25			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	CE_1 = High or CE_2 = Low, V_{OUT} = 5.5V			40			100	μA
		CE_1 = High or CE_2 = Low, V_{OUT} = 0.5V			-40			-100	
I_{OS}	Short circuit[3]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175		130	815	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V, CE_1 = High or CE_2 = Low		8			8		

AC ELECTRICAL CHARACTERISTICS

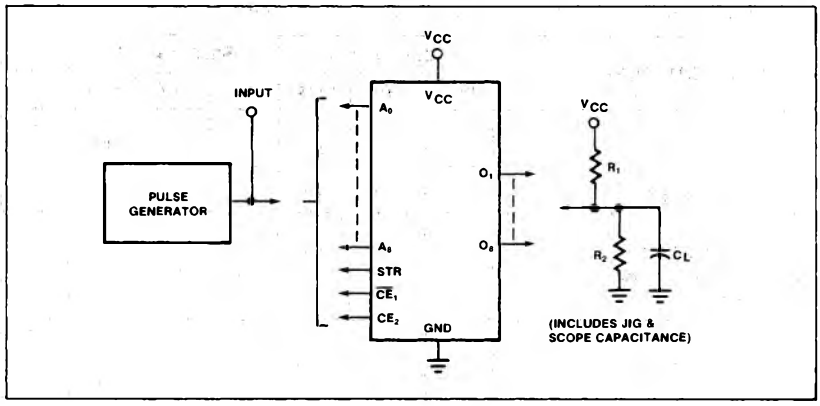
R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S214/215: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S214/215: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TO	FROM	TEST CONDITIONS	N82S214/215			S82S214/215			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time[4]			Latched or transparent read							ns
T_{AA}		Output	Address			35	60		35	90	
T_{CE}		Output	Chip enable			20	40		20	50	
	Disable time[4]			Latched or transparent read							ns
T_{CD}		Output	Chip disable			20	40		20	50	
	Setup and hold time[5]			Latched read only							ns
T_{ADH}	Hold time	Output	Address		0	-10		5	-10		
T_{CDS}	Setup time	Output	Chip enable		40			50			
T_{CDH}	Hold time				10	0		10	0		
	Pulse width[5]			Latched read only							ns
T_{SW}	Strobe				30	20		40	20		
	Latch time[5]			Latched read only							ns
T_{SL}	Strobe				60	35		90	35		
	Delatch time[5]			Latched read only							ns
T_{DL}	Strobe						30			35	

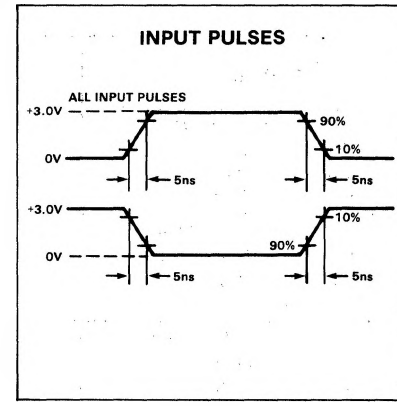
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
4. If the strobe is high, the device functions in a manner idential to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

TEST LOAD CIRCUIT

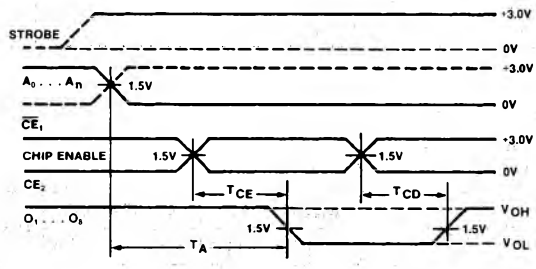


VOLTAGE WAVEFORM



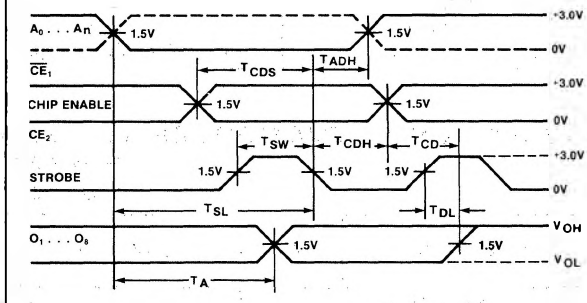
TIMING DIAGRAMS

TRANSPARENT READ



Output Latches Not Used

LATCHED READ



Output Latches Used