LB8107M



Portable CD Player Actuator Driver

Overview

The LB8107M is a portable CD player mechanism actuator driver. It operates on a 2.4 V power supply, which corresponds to two rechargeable Ni-Cd cells.

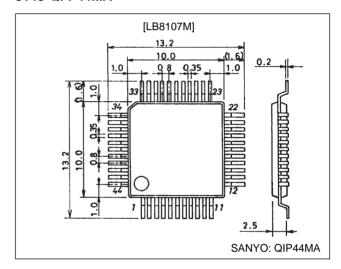
Functions and Features

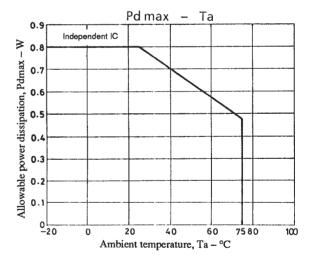
- Four H bridge driver channels on chip, one each for the four CD actuators; focus coil, tracking coil, spindle motor and sled motor
- Built-in step-up circuit to power the associated 5.0 V CD LSIs, including the DSP and microprocessor.
 (The drive transistor, L, Di and C are external components: step-up circuit) Io 150 mA, maximum
- Extremely low loss drive can be achieved, since the LB8107M detects the largest signal of the four drive channels and supplies that voltage to the H bridge driver blocks in each of the four channels using PWM voltage conversion.
 - (The drive PNP transistor, L, Di and C are external components: step-down circuit)
- System start and stop can be performed at the microprocessor output.
- Support for switching between step drive mode, which has a high current reduction effect, and normal V control for the sled motor drive (The other three channels all are V type drive only.)
- Built-in battery check comparator
- Built-in integrating amplifier to handle the application of digital servo control to earlier spindle motors (This function integrates the PWM output.)
- A defect function is provided. This function improves the tracking ability by setting the voltage supplied to the H bridge drivers to the maximum in the presence of disk defects during playback.

Package Dimensions

unit: mm

3148-QFP44MA





Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7.0	V
H bridge output current	I _{OUT}	Taking 400 mA/channel as the maximum.	800	mA
Step-up circuit output current	I _{CD}		150	mA
Allowable power dissipation	Pd max		800	mW
Operating temperature	Topr		-25 to +75	°C
Storage temperature	Tstg		-40 to +125	°C

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Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V _{CC}		2.0	2.4	4.0	V
Operating output				150		mW

Electrical Characteristics at $Ta=25^{\circ}C,\,V_{CC}$ = 2.4 V

Power Supply	Parameter	Symbol	Conditions	min	typ	max	Unit	
Standby current drain		Cymbol	Conditions		, typ	max	Offic	
Quiescent current 16C ma 18 27 ma (Sign-pur Circuit) VCD 4.775 5.0 5.25 V NPN translator drive current Inc 3.0 mA mA 1.00 mA 1.00 mM mA 1.00 mM mM 1.00 mM mM 1.00 mM		Icco	S/S1 = H. S/S2 = H			10	υΑ	
Step-up Circuit Output voltage	-		5,6. 1,6.62 1.		18		-	
Output voltage V _{CD} 4.76 5.0 5.25 V NPN Transitistor drive current Ino 3.0 mA 3.0 mA Voltage characteristics ΔV _{CD} /C _C 1.0 100 mV/V Minimum off duty 5.0 Voltage characteristics ΔV _{CD} /C _{CC} 100 mV/V Minimum off duty <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>								
NPN transistor drive current Inc		Vcp		4.75	5.0	5.25	V	
Voltage characteristics Δ°CO ^V CC		1			3.0		mA	
Voltage characteristics ΔV _{CD} /V _{CC} Monimum off duty 50 100 m/V/Monimum off duty Cossillator Circuit] Synchronization signal input frequency Fsvync 80 100 kHz Synchronization signal input frequency Fsvync 80 0 100 kHz HB Ridge Outputs] Saturation voltage Vcc (sat) 200 mA, TOP + BOTTOM 0.26 0.39 V Motor Control Biock] Imput voltage V _{IN} The linear region where V _{REF} 1 = 1/2 V _{CD} V _{REF} 1 V _{REF} 1 V _{REF} 1 V _L V Imput voltage V _{IN} The linear region where V _{REF} 1 = 1/2 V _{CD} V _{REF} 1 V _L V V Transmission gain (+) Gyrx 1.0 4.0	Load characteristics	ΔV _{CD} /I _{CD}				0.01	%/mA	
Minimum off duty Section Secti	Voltage characteristics	_				100	mV/V	
Synchronization signal input frequency Favync 80 100 kHz input frequency Hz Bridge Cuptus	Minimum off duty	02 00			50		%	
Favync	[Oscillator Circuit]							
Saturation voltage	1 -	Fsvync		80		100	kHz	
Motor Control Block	[H Bridge Outputs]	<u> </u>		<u>'</u>		•		
Input voltage	Saturation voltage	V _{CC} (sat)	200 mA, TOP + BOTTOM		0.26	0.39	V	
Input bias current IBDR	[Motor Control Block]			<u>'</u>		•		
Transmission gain (+) GyTR Within the same channel 7.95 dB	Input voltage	V _{IN}	The linear region where V _{REF} 1 = 1/2 V _{CD}		V _{REF} 1		V	
Transmission gain ratio (+)/(-) ΔG _{VTR} Within the same channel ±1 ±1 MR Input dead band voltage Vdz At the forward/reverse transition within a channel = ±10 mV Imput dead band voltage offset Vdzor At the forward/reverse transition within a channel = ±10 mV Imput dead band voltage offset Vdzor At the forward/reverse transition within a channel = ±20 ±10 mV Imput dead band voltage offset VQUT 2 2 7 V Maximum output voltage VQUT 1 2 2 2 7 V PNP transistor drive current Ipi * 2 0	Input bias current	I _{BDR}			1.0		μΑ	
Input dead band voltage Vdz Vdz At the forward/reverse transition within a channel Leg Le	Transmission gain (+)	G _{VTR}			7.95		dB	
Imput dead baind voltage Voltage At the forward/reverse transition within a channel At the forward/reverse transition At the forward/reverse t	Transmission gain ratio (+)/(-)	ΔG_{VTR}	Within the same channel		±1		dB	
PWM Maximum output voltage V _{OUT}	Input dead band voltage	Vdz					mV	
Maximum output voltage V_OUT 2.1 2.4 2.7 V PNP transistor drive current Ipi * V_OUT/600 mA Load characteristics ΔV_OUT/Ird 0.03 %/mA Voltage characteristics ΔV_OUT/VCc 0 0 50 mV/V Sled Drive Circuit] Drive Reference Voltage (step mode) V_REFO V_REFO V SLS on voltage V_SLS ON 2.0 V SLL input bias current I_BSLL 0 0 0 0 0 SLH input bias current I_BSLL 0 0 0 0 S/S Pins 1 and 2 P-on voltage V_DEF ON 0 2.0 V Reference Voltage V_DEF ON 0 0 0 0 Reference Voltage Pin 0 0 0 0 Cutput current V_REFO 0 0 0 0 Cutput voltage V_DEF ON 0 0 0 0 Cutput voltage V_DEF ON 0 0 0 0 Cutput voltage V_DEF ON 0 0 0 0 0 Cutput voltage V_DEF	Input dead band voltage offset	Vdzof	At the forward/reverse transition within a channel			±10	mV	
PNP transistor drive current Ipi *	[PWM]							
Load characteristics ΔV _{OUT} /Ird 0.03 %/mA Voltage characteristics ΔV _{OUT} /V _{CC} 50 mV/V [Sled Drive Circuit] Trive Reference Voltage (step mode) VREFO VREFO <td <="" rowspan="2" td=""><td>Maximum output voltage</td><td>V_{OUT}</td><td></td><td>2.1</td><td>2.4</td><td>2.7</td><td>V</td></td>	<td>Maximum output voltage</td> <td>V_{OUT}</td> <td></td> <td>2.1</td> <td>2.4</td> <td>2.7</td> <td>V</td>	Maximum output voltage	V _{OUT}		2.1	2.4	2.7	V
Voltage characteristics ΔV _{OUT} V _{CC} 50 mV/V [Sled Drive Circuit] Prive Reference Voltage (step mode) V _{REFO} <td <="" rowspan="2" td=""><td>PNP transistor drive current</td><td>lpi</td><td>*</td><td></td><td>V_{OUT}/600</td><td></td><td>mA</td></td>		<td>PNP transistor drive current</td> <td>lpi</td> <td>*</td> <td></td> <td>V_{OUT}/600</td> <td></td> <td>mA</td>	PNP transistor drive current	lpi	*		V _{OUT} /600	
Sled Drive Circuit] Drive Reference Voltage (step mode)	Load characteristics		$\Delta V_{OUT}/Ird$				0.03	%/mA
Drive Reference Voltage (step mode)	Voltage characteristics	ΔV _{OUT} /V _{CC}				50	mV/V	
SLS on voltage V _{SLS ON} 2.0 V	[Sled Drive Circuit]							
SLL input bias current I _{BSLH} 300 μA SLH input bias current I _{BSLH} 300 μA Defect voltage V _{DEF ON} 2.0 ν [S/S Pins 1 and 2] P-on voltage ν ν _{CC} - 1.0 ν P-off voltage ν ν ν [Reference Voltage Pin] Output current I _{REFO} 100 μA Output voltage ν _{REF} 2 1.2 ν [WP Pin] ν ν ν ν ν Battery Check Block] I _{BBI} 1.5 μA	_	V _{REFO}			V _{REF} 1 + 0.65		V	
SLL input bias current I _{BSLH} 300 μA SLH input bias current I _{BSLH} 300 μA Defect voltage V _{DEF ON} 2.0 ν [S/S Pins 1 and 2] P-on voltage ν ν _{CC} - 1.0 ν P-off voltage ν ν ν [Reference Voltage Pin] Output current I _{REFO} 100 μA Output voltage ν _{REF} 2 1.2 ν [WP Pin] ν ν ν ν ν Battery Check Block] I _{BBI} 1.5 μA	SLS on voltage	V _{SLS ON}		2.0			V	
Defect voltage V _{DEF ON} 2.0 V [S/S Pins 1 and 2] P-on voltage V _{CC} - 1.0 V P-off voltage V _{CC} - 0.5 V Reference Voltage Pin Output current I _{REFO} 1.2 V (WP Pin Output voltage V _{OPW} V _{OPW} V _{OPW} Battery Check Block BI input bias current I _{BBI} I 1.5 μA	SLL input bias current					300	μΑ	
See See	SLH input bias current	I _{BSLH}				300	μΑ	
P-on voltage	Defect voltage	V _{DEF ON}		2.0			V	
P-off voltage V _{CC} - 0.5 V [Reference Voltage Pin] V _{CC} - 0.5 V Output current I _{REFO} 100 μA Output voltage V _{REF} 2 1.2 V [WP Pin] V _{CD} 1 - 0.15 V V Battery Check Block] V _{OPW} 1.5 μA	[S/S Pins 1 and 2]							
Reference Voltage Pin	P-on voltage					V _{CC} – 1.0	V	
Output current I _{REFO} 100 μA Output voltage V _{REF} 2 1.2 V [WP Pin] Output voltage V _{OPW} V _{OPW} V _{OPW} V [Battery Check Block] Bl input bias current I _{BBI} 1.5 μA	P-off voltage			V _{CC} - 0.5			V	
Output voltage V _{REF} 2 1.2 V [WP Pin] V _{CD} 1 - 0.15 V Output voltage V _{OPW} V V [Battery Check Block] BI input bias current I _{BBI} 1.5 μA	[Reference Voltage Pin]							
[WP Pin] Output voltage	Output current	I _{REFO}				100		
Output voltage V _{OPW} V _{CD1} – 0.15 V [Battery Check Block] BI input bias current I _{BBI} 1.5 μA		V _{REF} 2			1.2		V	
Couput Voltage	[WP Pin]				T	ı		
Bl input bias current I _{BBI} 1.5 µA	Output voltage	V _{OPW}		V _{CD} 1 - 0.15			V	
	[Battery Check Block]							
BO output voltage V_{OBO} I_{OBO} = 500 μ A 0.3 V	BI input bias current	I _{BBI}				1.5	μA	
	BO output voltage	V _{OBO}	I _{OBO} = 500 μA			0.3	V	

Note: * This is a design guarantee and is not measured.

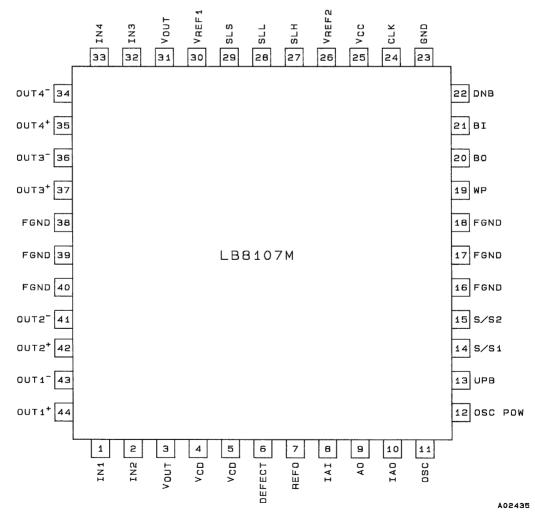
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Parameter	Symbol	Conditions	min	typ	max	Unit	
[CLK Block]	[CLK Block]						
CLK input voltage	V _{CLK}		2			V	
[Oscillator Block]							
Oscillator power voltage	V _{OSCP}		V _{CC} - 0.15			V	
OSC pin input bias current I _{BOSC}					-1.5	μA	
[Integrating Amplifier Block]	[Integrating Amplifier Block]						
Input bias current	I _{BIAI}				500	nA	
First stage amplifier gain	GV1	Open loop, f = 1 kHz*		55		dB	
Second stage amplifier gain	GV2	Internal closed loop		0		dB	
First stage output	V _O 1-1	1 mA SOURCE	V _{CD} – 1.3			V	
saturation voltage	V _O 1-2	1 mA SINK			1.3	V	
Second stage output	V _O 2-1	1 mA SOURCE	V _{CD} – 1.3			V	
saturation voltage	V _O 2-2	1 mA SINK			1.3	V	

Note: * This is a design guarantee and is not measured.

Pin Assignment



Top view

Pin Functions Unit (resistance: Ω)

			Unit (resistance: Ω)
Pin No.	Symbol	I/O	Pin function
1	IN1	1	Actuator control input: focus
2	IN2	ı	Actuator control input: tracking
3, 31	V _{OUT}		Power supply for the four H bridge channels
4, 5	V _{CD}	I	Step-up circuit output voltage
6	DEFECT	I	Sets V _{OUT} to its maximum voltage on defect input. VCC 50 # A A02425
7	REFO	0	Sled drive reference voltage
8	IAI		Integrating amplifier input
9	AO	0	Inverting amplifier output
10	IAO		Integrating amplifier output
11	osc		Free-running oscillator: RC circuit connection
12	OSCPOW	0	Free-running oscillator: RC circuit power supply
13	UPB	0	Step-up npn transistor drive output VCC A02425
14	S/S1	I	Starts the system when a low level is applied as the LB8107M start input (power on lock from the microprocessor) VCC A02427
15	S/S2	I	Provides a logical or function with the S/S1 input (for starting from a switch input) VCC A02428

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Unit (resistance: Ω)

			Unit (resistance: \(\frac{1}{2}\)
Pin No.	Symbol	I/O	Pin function
16, 17, 18, 38, 39, 40	FGND		Ground for the power block
			Microprocessor start-up output linked to S/S2. pnp open collector output
19	WP	0	V _{CD1} (5pin)
			Battery low output. npn open collector output; Low: battery low
20	во	o	A02430
			Battery voltage detection pin
21	ВІ	1	200 VCC
			Voltage reduction pnp transistor drive output
22	DNB	0	VCC VCC
23	GND		Signal ground
24	CLK	I	External clock input pin VCC SOMA BOK BOK A02433
25	V _{CC}		Power supply: 2.0 to 4.0 V
26	V _{REF} 2		Reference voltage: 1.2 V
27	SLH	ı	Sled drive starting voltage adjustment

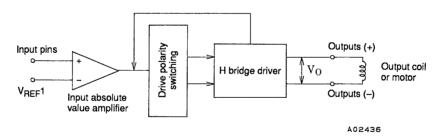
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Unit (resistance: Ω)

Pin No.	Symbol	I/O	Pin function
28	SLL	ı	Sled drive stop voltage adjustment
29	SLS	I	Sled switching VCC 50 # A A02434
30	V _{REF} 1	I	Motor control block input reference voltage: supplied from the CD servo IC
32	IN3	I	Actuator control input: Spindle
33	IN4	ı	Actuator control input: Sled
34	OUT4 (-)	0	Actuator control output (–): Sled
35	OUT4 (+)	0	Actuator control output (+): Sled
36	OUT3 (–)	0	Actuator control output (–): Spindle
37	OUT3 (+)	0	Actuator control output (+): Spindle
41	OUT2 (–)	0	Actuator control output (–): Tracking
42	OUT2 (+)	0	Actuator control output (+): Tracking
43	OUT1 (–)	0	Actuator control output (–): Focus
44	OUT1 (+)	0	Actuator control output (+): Focus

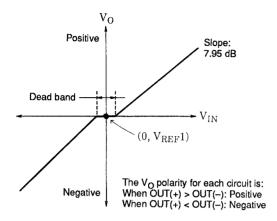
Functional Description

1. Actuator drivers (focus, tracking, spindle and sled)



 $V_{REF}1$ is supplied from the CD DSP that is powered by the stepped-up voltage (5.0 V) created by the LB8107M. (Normally, $V_{REF}1$ will be $1/2\ V_{CD}2$.)

The figure below shows the form of the I/O transmission characteristics.



That is, the LB8107M implements a polarity reversing V-type drive with respect to the input signals (from the DSP) referenced to $V_{REF}1$.

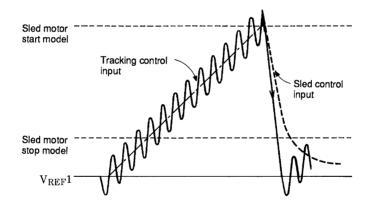
The transmission gain $\Delta V_O/\Delta V_{IN}$ is 7.95 (typical) and the LB8107M provides a region (dead band) around $V_{REF}1$ where the output does not change with the input. (The dead band is $V_{REF}1\pm100~mV$ (maximum).)

The LB8107M provides excellent gain precision since the a feedback structure is adopted in the drive circuits.

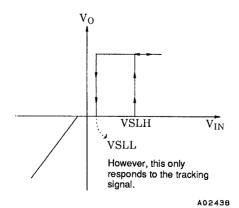
2. Sled motor step drive switching (selected when the SLS pin is low)

While it goes without saying that the V-type drive described above can be used for sled motor drive, the LB8107M also supports a step drive scheme to reduce sled motor drive power.

Since a signal that is generated by integrating the tracking output is usually used as the sled motor control input, step drive attempts to drive the sled motor only during certain periods by providing a sled motor start command from the sled motor control input and a sled motor stop command from the tracking control input.



The start and stop levels are set by an external resistor connected between the $V_{REF}1$ pin and the REFO pin.



Note that for inputs that are lower than $V_{REF}1$ this system operates normally regardless of the SLS pin.

Also, as will be discussed later, the maximum voltage is supplied to the H bridge in step drive mode.

3. Step-up Circuit

The step-up circuit can be used to power not only the four driver channel control stages, but also external circuits. (V_{DD} is 5.0 V (typical) with an Io of 150 mA (maximum).)

This step-up circuit operates from the built-in oscillator's free-running mode immediately after the system is started.

(The frequency is determined by the RC circuit connected to the OSCP* pin. When C is 400 pF and R is 30 k Ω , the frequency will be about 80 kHz.)

Note: * This pin is used for current pass prevention in standby mode.

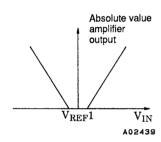
After the system is started, (to bring up the CD DSP and other circuits) when a clock with a frequency (e.g., 2fc = 88.2 kHz) greater than the free-running frequency is input to the CLK pin, the oscillator synchronizes with the input clock. \rightarrow frequency only synchronization. (Since the frequency range is from 80 to 100 kHz, 88.2 kHz is optimal as the input frequency.)

Since the on/off duty ratio is set to have a maximum of 50%, i.e., the on period ranges from 0 to 50%, this provides a protection function for the output transistors when large loads are applied. (We strongly recommend using output transistors with an h_{FE} as large as possible. Also, for efficiency, we recommend using Schottky diodes.)

4. PWM Power Supply Scheme

To improve power efficiency as much as possible in the LB8107M, maximum value output PWM voltage conversion is used in the power supply for each of the four H bridge driver channels.

5. The maximum value of the control block outputs (the outputs of the absolute value amplifiers with respect to their



inputs) for each of the drivers is detected, and a voltage consisting of that voltage plus a margin (the offset) is supplied to the H bridge for each channel using PWM voltage conversion (step-down converter). (This allows the actuators to be driven with the minimum power in cases such as, for example, when the operating voltages for all four actuator channels are identical and small.) Unlike schemes in which a PWM converter is provided for each channel, only one L/C pair is required, and furthermore, since the actuator drive is linear, this scheme does not generate the noise levels associated with direct PWM schemes. Also, since the voltage supplied to the H bridges by this PWM scheme is limited to 2.4 V (typical), there are no

changes in the maximum currents supplied to the actuators associated with changes in the power supply voltage used. Furthermore, this scheme is designed so that the maximum voltage is supplied when the defect signal from the DSP, which indicates the presence of defects, is high or when in sled motor step drive mode.

6. System Start and Stop Commands

The LB8107M is designed so that the system can be started and stopped by the control microprocessor.

[Start]

The pins S/S1 and S/S2 are provided as system startup pins. Of these, S/S1 locks the system power supply when it is set low by the microprocessor as a power on lock. S/S2 is provided to be used for startup from a switch and the function operates by taking the logical with S/S1. However, the microprocessor can still apply the S/S1 power on lock by reading the WP (wake up) pin output, since this output is goes high when S/S2 is low.

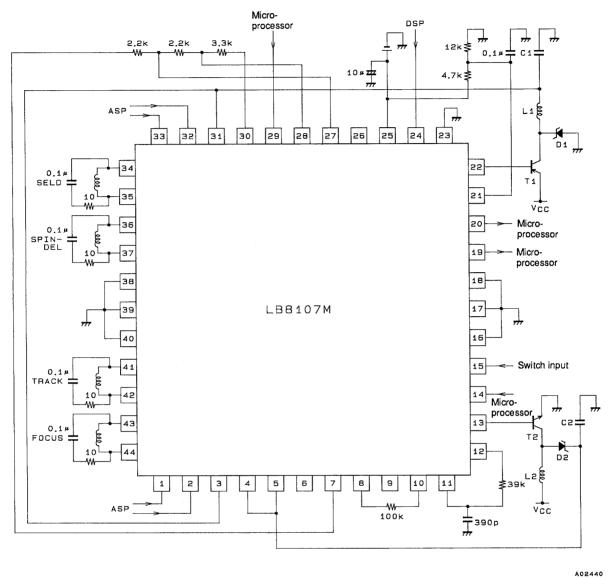
[Stop]

The system power supply can be shut down by setting both S/S1 and S/S2 high. This puts the LB8107M in standby mode.

[Other notes]

- ullet Circuit blocks that use $V_{CD}1$ as the power supply Integrating amplifier, inverting amplifier, sled switching circuit (including SLS, SLH and SLL) and the maximum value circuit
- Circuit blocks that use V_{CC} as the power supply
 Step-up circuit, step-down circuit, reference voltage, battery check, oscillator, edge start and other circuits.

Sample Application Circuit



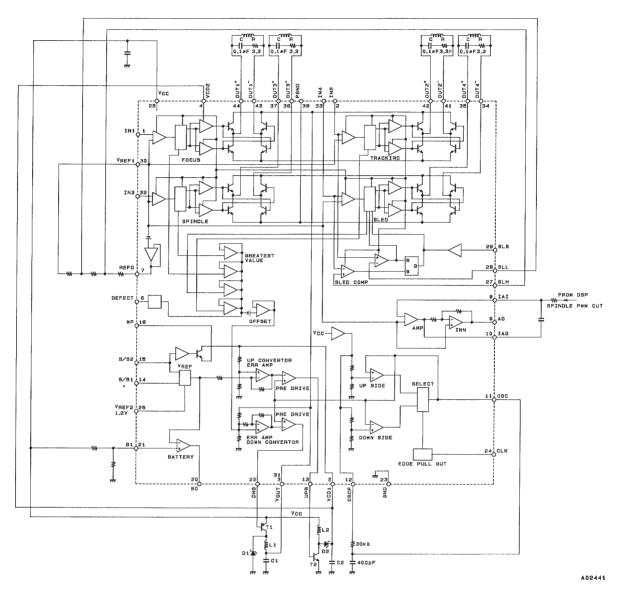
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Unit (resistance: Ω , capacitance: F)

T1	2SB815
T2	2SC3650
D1 = D2	SB07-03C
L1 = L2	30 µH
C1 = C2	100 µF

To control the spindle motor using a digital servo scheme, input the PWM output to pin 8, set up the external integration constant, and input the output from pin 9 to the spindle input.

Internal Equivalent Circuit



Reference values Unit (resistance: Ω)

T12SB815 T22SC3650 D1 = D2SB07-03C L1 = L230 μH (under 1.35 Ω , 600 mA) C1 = C2100 μF

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