Monolithic Digital IC



# LB8901M

# **CCD Clock Driver**

## Overview

The LB8901M is a monolithic IC designed to drive largecapacity clock gates of a CCD image sensor (LC9900 series) at a high speed.

### Features

- Capable of driving large-capacity gates of a CCD, etc.
- On-chip eight-block driver, two of which are capable of providing drive on the three-value level (LC9900 series).
  No more than one chip is required to drive vertical gates.
- Placed in a 24-pin miniflat package (MFP24S), facilitating miniaturization of equipment.
- Capable of being driven direct with TTL, CMOS, etc.
- A power save circuit can be connected to permit less power dissipation.

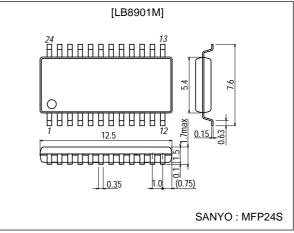
## **Specifications**

#### Absolute Maximum Ratings at $Ta = 25^{\circ}C$

## **Package Dimensions**

## unit:mm

#### 3112A-MFP24S



Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max	Each V <sub>CC</sub> pin	-0.3 to +18.0	V
Input supply voltage	VIN	Each input pin	-0.3 to +6.0	V
Maximum output current	IOUT	Each output pin	250	mA
Allowable power dissipation	Pd max		620	mW
Operating temperature	Topr		-10 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

#### Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VCC	Each V <sub>CC</sub> pin	5 to 18	V
Supply voltage	$\Delta V_{CC}$ 1-2	V <sub>CC</sub> 1–V <sub>CC</sub> 2 voltage difference	0 to 6.0	V
Input high-level voltage	$V_{H}$	Each input pin	2.5 to 6.0	V
Input low-level voltage	VIL	Each input pin	-0.3 to +0.3	V

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## **Electrical Characteristics** at Ta = 25°C, $V_{CC}$ 1=9.0V, $V_{CC}$ 2 to 5=13.0V

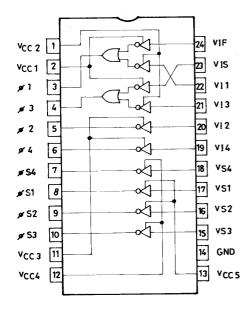
Parameter	Symbol	Symbol Conditions	Ratings			Unit
Parameter	Symbol		min	typ	max	Unit
	I <sub>IH</sub> 1	VI1, VI3 inputs of blocks 1, 2, VIN=5.0V		1.0	2	mA
Input high-level current	I <sub>IH</sub> 2	VIF, VIS inputs of blocks 1, 2, VIN=5.0V		1.0	2	mA
	I <sub>IH</sub> 3	V <sub>I</sub> 2, V <sub>I</sub> 4 inputs of blocks 3, 4, V <sub>IN</sub> =5.0V		1.0	2	mA
	I <sub>IH</sub> 4	$V_{S}$ 1 to 4 inputs of blocks 5 to 8, $V_{IN}$ =5.0V		1.0	2	mA
Input low-level current	I <sub>IL</sub> 1	$V_{I}1$ to 4, $V_{S}1$ to 4 inputs of blocks 1 to 8, $V_{IN}{=}0V$	-30			μA
	I <sub>IL</sub> 2	$V_{IF}$ , $V_{IS}$ inputs of blocks 1, 2, $V_{IN}$ =0V	-100	-20		μΑ
	ICCH1	Each input ; V <sub>IN</sub> =5.0V		0.5	1	mA
	ICCH <sup>2</sup>	Each input ; V <sub>IN</sub> =5.0V		4.0	8	mA
	ICCH3	Each input ; V <sub>IN</sub> =5.0V		4.0	8	mA
	ICCH4	Each input ; V <sub>IN</sub> =5.0V		4.0	8	mA
Supply current	ICCH <sup>5</sup>	Each input ; V <sub>IN</sub> =5.0V		4.0	8	mA
Supply current	I <sub>CCL</sub> 1	Each input ; V <sub>IN</sub> =0V			300	μA
	I <sub>CCL</sub> 2	Each input ; V <sub>IN</sub> =0V			100	μA
	I <sub>CCL</sub> 3	Each input ; V <sub>IN</sub> =0V			100	μΑ
	I <sub>CCL</sub> 4	Each input ; V <sub>IN</sub> =0V			100	μΑ
	I <sub>CCL</sub> 5	Each input ; V <sub>IN</sub> =0V			100	μΑ
Output voltage	V <sub>OH</sub> 1	V <sub>I</sub> 1=0V, V <sub>IF</sub> =5V	V <sub>CC</sub> 2–2.0			V
	V <sub>OH</sub> 2	VI1=0V, VIF=0V	V <sub>CC</sub> 1–1.0			V
	V <sub>OH</sub> 3	V <sub>I</sub> 3=0V, V <sub>IS</sub> =5V	V <sub>CC</sub> 2–2.0			V
	V <sub>OH</sub> <sup>4</sup>	V <sub>I</sub> 3=5V, V <sub>IS</sub> =0V	V <sub>CC</sub> 1–1.0			V
	V <sub>OH</sub> 5	V <sub>1</sub> 2, V <sub>1</sub> 4=0V	V <sub>CC</sub> 3–2.0			V
	V <sub>OH</sub> 6	V <sub>S</sub> 3, V <sub>S</sub> 4=0V	V <sub>CC</sub> 4–2.0			V
	V <sub>OH</sub> 7	V <sub>S</sub> 1, V <sub>S</sub> 2=0V	V <sub>CC</sub> 5–2.0			V
	V <sub>OL</sub>	Each input V <sub>IN</sub> =5V			1.0	V

### Switching Characteristics at Ta = 25°C, V<sub>CC</sub>1=9.0V, V<sub>CC</sub>2 to 5=13.0V, V<sub>IN</sub>=5.0V, t<sub>r</sub>, t<sub>f</sub>≤10ns

Parameter	Symbol	Conditions	Ratings			Unit
Parameter	Symbol		min	typ	max	Unit
	t <sub>PLH</sub> 1	ø1, 3 outputs ; V <sub>IF</sub> , V <sub>IS</sub> =5.0V fixed		30		ns
Propagation time low-level $\rightarrow$ high-level	tPLH <sup>2</sup>	ø1, 3 outputs ; V <sub>I</sub> 1, V <sub>I</sub> 3=5.0V fixed		2		μs
	tPLH3	ø2, 4, øS1 to 4 outputs		30		ns
	t <sub>PHL</sub> 1	ø1, 3 outputs ; V <sub>IF</sub> , V <sub>IS</sub> =5.0V fixed		30		ns
Propagation time high-level $\rightarrow$ low-level	tPHL2	ø1, 3 outputs ; V <sub>I</sub> 1, V <sub>I</sub> 3=5.0V fixed		1		μs
	tPHL3	ø2, 4, øS1 to 4 outputs		30		ns
	t <sub>r</sub> 1	ø1, 3 outputs ; V <sub>IF</sub> , V <sub>IS</sub> =5.0V fixed		30		ns
Transient rise time	t <sub>r</sub> 2	ø1, 3 outputs ; V <sub>I</sub> 1, V <sub>I</sub> 3=5.0V fixed		6		μs
	t <sub>r</sub> 3	ø2, 4, øS1 to 4 outputs		30		ns
	t <sub>f</sub> 1	ø1, 3 outputs ; V <sub>IF</sub> , V <sub>IS</sub> =5.0V fixed		30		ns
Transient fall time	t <sub>f</sub> 2	ø1, 3 outputs ; V <sub>I</sub> 1, V <sub>I</sub> 3=5.0V fixed		300		ns
	t <sub>f</sub> 3	ø2, 4, øS1 to 4 outputs		30		ns

Note : Load conditions

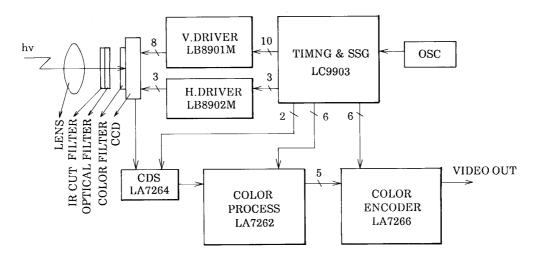
#### **Equivalent Circuit Block Diagram**



#### **Pin Function**

Pin No.     Pin Name     Pin Description       1     V <sub>CC</sub> 2     Power supply for frame shift pulse at ø1, 3       2     V <sub>CC</sub> 1     Power supply for three-value pulse at ø1, 3       3     ø1     Positive three-value drive output, for ø1 of CCI       4     ø2     Positive three-value drive output, for ø3 of CCI       5     ø3     Positive two-value drive output, for ø2 of CCD       6     ø4     Positive two-value drive output, for ø4 of CCD	
2     V <sub>CC</sub> 1     Power supply for three-value pulse at ø1, 3       3     ø1     Positive three-value drive output, for ø1 of CCI       4     ø2     Positive three-value drive output, for ø3 of CCI       5     ø3     Positive two-value drive output, for ø2 of CCD	
3     Ø1     Positive three-value drive output, for Ø1 of CCI       4     Ø2     Positive three-value drive output, for Ø3 of CCI       5     Ø3     Positive two-value drive output, for Ø2 of CCD	
4ø2Positive three-value drive output, for ø3 of CCI5ø3Positive two-value drive output, for ø2 of CCD	
5 ø3 Positive two-value drive output, for ø2 of CCD	D
6 Ø4 Positive two-value drive output for Ø4 of CCD	
7 ØS4 Positive two-value drive output, for ØS4 of CCE	)
8 ØS1 Positive two-value drive output, for ØS1 of CCE	C
9 ØS2 Positive two-value drive output, for ØS2 of CCE	C
10 ØS3 Positive two-value drive output, for ØS3 of CCE	C
11 V <sub>CC</sub> 3 Power supply for ø2, 4	
12 V <sub>CC</sub> 4 Power supply for øS3, S4	
13 V <sub>CC</sub> 5 Power supply for øS1, S2	
14 GND Ground pin	
15 V <sub>S</sub> 3 Clock input for øS3 driver	
16 V <sub>S</sub> 2 Clock input for øS2 driver	
17 V <sub>S</sub> 1 Clock input for øS1 driver	
18 V <sub>S</sub> 4 Clock input for øS4 driver	
19 V <sub>I</sub> 4 Clock input for ø4 driver	
20 V <sub>1</sub> 2 Clock input for ø2 driver	
21 V <sub>1</sub> 3 Clock input for ø3 driver	
22 V <sub>1</sub> 1 Clock input for ø1 driver	
23 V <sub>IS</sub> Three-value pulse input for ø3 driver	
24 VIF Three-value pulse input for ø1 driver	

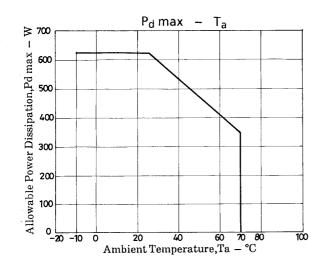
#### Sample Application Circuit : Camera Block Diagram



#### Proper Cares to be Taken in Designing a Printed Circuit Board

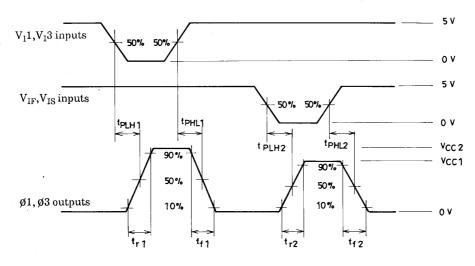
The LB8901M draws a large instantaneous current when it drives a load. The LB8901M is also designed to drive a load at a very high speed. When designing a printed circuit board, keep in mind the following points to prevent the output waveforms from being adversely affected.

- 1) Make the pattern of the power supply, GND lines as large as possible.
- 2) Place the bypass capacitor as close to the IC as possible (less than 1cm).
- 3) Make the wiring of the input signal line as short as possible to minimize the effect of stray capacitance.
- 4) Make the wiring of the output signal line also as short as possible, because the inductance of a long signal line may affect the output waveforms adversely.
- Take such necessary measures that a small resistance is inserted in series with a load.
- 5) When using a power save circuit, place it also as close to the IC as possible.



#### **Switching Waveforms**

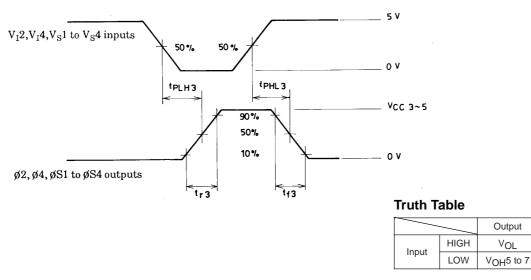
1) Blocks 1, 2



**Truth Table** 

$\sim$		VIF, VIS inputs		
		HIGH	LOW	
V <sub>I</sub> 1, V <sub>I</sub> 3 Input	HIGH	VOL	V <sub>OH</sub> 2, 4	
İnput	LOW	V <sub>OH</sub> 1, 3	Inhibit	

2) Blocks 3 to 8



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