

# LC651204N/F/L,LC651202N/F/L

## 4-Bit Single-Chip Microcontroller for Small-Scale Control Applications

## Preliminary

## Overview

The LC651204N/F/L and LC651202N/F/L are small-scale application microcontroller products in Sanyo's LC6500 series of 4-bit single-chip CMOS microcontrollers, and as such they fully support the basic architecture and instruction set of that series. These microcontrollers are provided in a 30-pin package and include 2 kilobytes (KB) and 4 KB of on-chip ROM. These products are appropriate for use in a wide range of applications, from applications that use a small number of controls and circuits that were previously implemented in standard logic to larger scale applications including audio equipment such as decks and players, office equipment, communications equipment, automotive equipment, and home appliances. Except for the lack of an A/D converter, these microcontrollers provide the same functionality as the LC651104, 02N/F/L.

### Features

(2) ROM/RAM

- (1) Fabricated in a CMOS process for low power (An instruction-controlled standby function is provided.)
  - LC651204N/F/L ROM:  $4K \times 8$  bits, RAM:  $256 \times 4$  bits
    - LC651202N/F/L ROM:  $2K \times 8$  bits, RAM:  $256 \times 4$  bits
- (3) Instruction set: The 80-instruction set provided by all members of the LC6500 series.
- (4) Wide operating power-supply voltage range of 2.5 to 5.5 volts (L version)
- (5) Instruction cycle time: 0.92µs (F version)
- (6) On-chip serial I/O circuit
- (7) Highly flexible I/O ports
  - Number of ports: 6 ports with a total of 22 pins
  - All ports: Can be used for both input and output
    - I/O voltage: 15V maximum (Only for C, D, E, and F ports with open-drain output specifications) Output current: 20mA maximum sink current (Capable of directly driving LEDs.)

Options that allow specifications to be customized to match those of the application system.
 Specification of open-drain output or built-in pull-up resistor: Can be specified for all ports in bit units.
 Specification of the output level at reset: Can be specified to be high or low for ports C and D in port units.

- (8) Interrupt functions
  - Timer overflow vector interrupt (The interrupt state can be tested by the CPU.)
  - Vector interrupts initiated by the INT pin or full/empty states of the serial I/O circuit. (The interrupt state can be tested by the CPU.)
- (9) Stack levels: 8 levels (shared with interrupts)
- (10) Timers: 4-bit prescaler plus 8-bit programmable timers
- (11) Clock oscillator options to match application system specifications.
  - Oscillator circuit options: 2-pin ceramic oscillator (N, F and L versions)
- Divider circuit option: No divider, built-in divide-by-three circuit, built-in divide-by-four circuit (N and L versions)
- (12) Supports continuous output of a square wave signal (with a period 64 times the cycle time)
- (13) Watchdog timer
  - RC time constant scheme
- A watchdog timer function can be allocated to one of the external pins as an option.
- (14) EP version: LC65E1104, OTP version: LC65P1104
  - Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
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#### Package Dimensions

[LC651204N/F/L, 651202N/F/L]

(unit : mm) 3073A (unit : mm) 3196A

[LC651204N/F/L, 651202N/F/L]



SANYO : MFP-30S

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SANYO : DIP-30SD
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#### [Notes]

The package drawings shown above are provided without error tolerances and are for reference purposes only. Contact Sanyo for official package drawings.

	Item	LC651204N/1202N	LC651204F/1202F	LC651204L/1202L	
Memory	ROM	4096×8 bits(1204N)	4096×8 bits(1204F)	4096×8 bits(1204L)	
		2048×8bits(1202N)	2048×8 bits(1202F)	2048×8 bits(1202L)	
	RAM	256×4 bits(1204/1202N)	256×4 bits(1204/1202F)	256×4 bits(1204/1202L)	
Instruction	Instruction set	80	80	80	
	Table reference	Supported	Supported	Supported	
Built-in functions	Interrupts	1 external, 1 internal	1 external, 1 internal	1 external, 1 internal	
	Timers	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer	
	Stack levels	8	8	8	
	Standby function	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction	
I/O ports	Number of ports	22 I/O pins	22 I/O pins	22 I/O pins	
-	Serial ports	4-bit or 8-bit I/O	4-bit or 8-bit I/O	4-bit or 8-bit I/O	
	I/O voltage	15V max.	15V max.	15V max.	
	Output current	10mA typ. 20mA max.	10mA typ. 20mA max.	10mA typ. 20mA max.	
	I/O circuit types	Open drain (n-channel) or built -in pull-up resistor output selectable on a per-bit basis.			
	Output levels at reset	High or low can be selected in port units. (ports C and D only)			
	Square wave output	Supported	Supported	Supported	
Characteristics	Minimum cycle time	2.77µs (VDD≥3V)	0.92µs (VDD≥3V)	3.84µs (VDD≥2.5V)	
	Power-supply voltage	3 to 5.5V	3 to 5.5V	2.5 to 5.5V	
	Power-supply current	1.5mA typ.	2mA typ.	1.5mA typ.	
Oscillator	Oscillator	Ceramic (800K, 1MHz, 4MHz)	Ceramic (4MHz)	Ceramic (800K, 1MHz, 4MHz)	
	Divider circuit option	1/1, 1/3, 1/4	1/1	1/1, 1/3, 1/4	
Other functions	Package	DIP30S-D MFP30S	DIP30S-D MFP30S	DIP30S-D MFP30S	

#### **Function Overview**

[Notes]

Sanyo will announce details on oscillator elements and oscillator circuit constants as recommended application circuits are developed. Customers should check with Sanyo for the latest information as the development process progresses.

## **Pin Assignment**

Common assignments for the DIP and MFP packages



[Notes] NC pins must be connected to VSS.

Top view

## **Pin Functions**

Pin	Function
OSC1, OSC2	Connections for a ceramic oscillator element
RES	Reset
PA0 to 3	I/O dual-function port A0 to A3
PC0 to 3	I/O dual-function port C0 to C3
PD0 to 3	I/O dual-function port D0 to D3
PE0 to 1	I/O dual-function port E0 to E1
PF0 to 3	I/O dual-function port F0 to F3
PG0 to 3	I/O dual-function port G0 to G3
TEST	Test
ĪNT	Interrupt request
SI	Serial input
SO	Serial output
SCK	Serial clock input and output
NC	No connection
WDR	Watchdog reset

[Notes]

The SI, SO,  $\overline{\text{SCK}}$  and  $\overline{\text{INT}}$  pins are shared function pins that are also used as PF0 to PF3.

## System Block Diagram

PA0-3 (L) Port A RAM PC ROM F WR I/O Buffer STACK 1 to DP STACK 8 I.DEC IR PG0-3 ( Port G PC0-3 Port C System Bus 红子 €€ Port D PD0-3 Е AC STS ZF extf<u>t</u>mf ΤM CF CSF ZSF Serial shift register INT PF1/SOo Serial Serial 4/8 bit ŝ mode mode OSC OSC1 register register Shared with port F →OOSC2 lower digit ſ • RES I/O Bus Serial হ হ • TEST 4 bit shift -o VDD register Port E Port F -o VSS higher digit PF0/SIo হি ᡬᡷ γ 4/8 bit PF2/SCK o↔ WDR PF0-3 PE0-1 --- PF3/INT O

LC651204N/F/L, LC651202N/F/L

- RAM : Data memory
  - F : Flag
- WR : Working register
- AC : Accumulator
- ALU : Arithmetic and logic unit
- DP : Data pointer
- E : E register
- CTL : Control register
- OSC : Oscillator circuit
- TM : Timer
- STS : Status register

- ROM : Program memory
  - PC : Program counter
- INT : Interrupt control
- IR : Instruction register
- I.DEC : Instruction decoder
- CF, CSF : Carry flag, carry save flag
- ZF, ZSF : Zero flag, zero save flag
  - EXTF : External interrupt request flag
  - TMF : Internal interrupt request flag

## **Development Support**

Sanyo provides the following items to support application development using the LC651204 and LC651202.

1. User's manual

The "LC651104/1102 User's Manual" is used with these microcontrollers.

- 2. Development tool manual
- See the "EVA800-LC651104/1102 Development Tool Manual" for details on use of the EVA-800 system.
- 3. Development tool
  - Program development (using the EVA-800 system)
    - MS-DOS host computer system \*1
    - Cross assembler ... MS-DOS-based cross assembler: LC65S.EXE
    - Evaluation chip: LC6595
    - Emulator: The EVA-800 main unit plus the evaluation chip
  - Program development (using the EVA-800 system): Use the EVA86K-ECB651100.
  - Program evaluation
    - The <LC65E1104> on-chip EPROM microcontroller

## **Development Support System**

EVA-800 System



#### [Notes]

- 1. MS-DOS is a registered trademark of Microsoft Corporation
- 2. Here, "EVA-800" is a generic tem for several emulators. Suffixes (A, B, etc.) will be attached to the name as new versions are developed. Note that the EVA-800 emulator (i.e., the model with no suffix) is an old version and cannot be used.

## **Pin Functions**

Pin	Pin no.	I/O	Function	Option	State at reset	Handling when unused
VDD	1	-	Power supply	-	-	-
VSS	1	-				
OSC1	1	Input	System clock oscillator	(1) External clock	-	-
OSC2	1	Output	Connect an external ceramic	(2) Two-pin ceramic oscillator		
			oscillator element to these pins	(3) Divider circuit option		
			• Leave OSC2 open if an external	1. No divider circuit		
			clock is supplied.	2. Divide-by-three circuit		
				3. Divide-by-four circuit		
PA0	4	I/O	• I/O port A0 to A3	(1) Output open drain	High-level output	Open drain output
to			Input in 4-bit units using the IP	(2) Built-in pull-up resistor	(i.e., the output	select the options,
PA3			instruction	• Options (1) and (2) can be	n-channel transistor will	connect to VSS
			Output in 4-biit units using the OP	specified in bit units.	be off.)	
			Port hits can be tested in hit units			
			using the BP and BNP			
			instructions			
			Port hits can be set or cleared in hit			
			units using the SPB and RPB			
			instructions.			
			• PA3 is used for standby control.			
			• Applications must be designed so			
			that no chattering (e.g. switch			
			bounce) occurs on the PA3 pin			
			during a HALT instruction			
			execution cycle.			
PC0	4	I/O	• I/O port C0 to C3	(1) Output open drain	High-level output	The same as PA0 to
to			The PC0 to PC3 pin functions	(2) Built-in pull-up resistor	Low-level output	PA3.
PC3			are identical to those of the	(3) High-Level output at reset	(Depending on the option	
			PA0 to PA3 pins. *	(4) Low-Level output at reset	specified.)	
			• High or low can be specified as the	• Options (1) and (2) can be		
			output at reset as an option.	specified in bit units		
			Note: These pins do not have	• Options (3) and (4) are specified		
			a standby control function.	in 4-bit units		
PD0	4	I/O	• I/O port D0 to D3	The same as PC0 to PC3.	The same as PC0 to PC3.	The same as PA0 to
to			The PD0 to PD3 pin functions and			PA3.
PD3			options are identical to those of the			
			PC0 to PC3 pins.			

Pin	Pin no.	I/O	Function	Option	State at reset	Handling when unused
PE0 to PE1 /WDR	2	Ϊ́Ο	<ul> <li>I/O port E0 to E1 Input in 4-bit units using the IP instruction Output in 4-biit units using the OP instruction Port bits can be set or cleared in bit units using the SPB and RPB instructions. Port bits can be tested in bit units using the BP and BNP instructions.</li> <li>The PE0 pin also has a continuous pulse (64-Tcyc) output function.</li> <li>The PE1 pin can be set to function as the WOR watchdog timer reset pin as an option</li> </ul>	<ol> <li>Output open drain</li> <li>Built-in pull-up resistor         <ul> <li>Options (1) and (2) can be specified in bit units.</li> <li>Normal port PE1</li> <li>Watchdog timer reset WDR</li> <li>(3) or (4) can be specified.</li> </ul> </li> </ol>	High-level output (i.e., the output (ii.n-channel transistor will be off.)	The same as PA0 to PA3.
PF0/SI PF1/SO PF2/ SCK PF3/ INT	4	ΙΟ	<ul> <li>Watchdog timer reset pin as an option.</li> <li>I/O port F0 to F3 This port has the same functions and options as PE0 to PE1. * </li> <li>The pins PF0 to PF3 are also used as the serial interface and the INT pin.</li> <li>The function used can be selected under program control. SI Serial input port SO Serial input port SCK Serial clock input or output INT Interrupt request input Serial I/O can be switched between 4-bit and 8-bit operation under program control. Note: This port does not provide a continuous pulse output function.</li></ul>	The same as PA0 to PA3.	The same as PA0 to PA3. The serial port function is disabled. The interrupt source is INT.	The same as PA0 to PA3.
PG0 to PG3	4	I/O	<ul> <li>I/O port G0 to G3         This port has the same functions and options as PE0 to PE1. *         Note: This port does not provide a continuous         mulae output function     </li> </ul>	The same as PA0 to PA3.	The same as PA0 to PA3.	The same as PA0 to PA3.
NC	2		NC pin. This pin must be connected     to VSS in the EP and OTP versions	-	-	Connect to VSS.
RES	1	Input	<ul> <li>System reset input</li> <li>Connect an external capacitor for the power up reset.</li> <li>A low level must be applied for at least four clock cycles for the reset startup sequence to operate correctly.</li> <li>I SI test nin</li> </ul>	-	-	- Must be connected to
1251	1	mput	• Lot test pin Must be connected to VSS.	-	-	VSS.

## **Oscillator Circuit Options**

Option	Circuit	Conditions and notes
External clock		The OSC2 pin must be left open.
Ceramic oscillator	C1 OSC1 TT Ceramic oscillato element TT C2 R	

## **Divider Options**

Option	Circuit	Conditions and notes
No divider (1/1)	Oscillator circuit 750 700 700 700 700 700	<ul> <li>Supports both oscillator options.</li> <li>The oscillator frequency or the external clock frequency must not exceed 1444 kHz (LC651204N and LC651202N)</li> <li>The oscillator frequency or the external clock frequency must not exceed 4330 kHz (LC651204F and LC651202F)</li> <li>The oscillator frequency or the external clock frequency must not exceed 1040 kHz (LC651204L and LC651202L)</li> <li>Supports both oscillator entions</li> </ul>
Built-in divide-by-three circuit	fOSC initia bio de bio	<ul> <li>Supports both oscillator options.</li> <li>The oscillator frequency or the external clock frequency must not exceed 4330 kHz</li> </ul>
Built-in divide-by-four circuit	fOSC timing generator	<ul> <li>Supports both oscillator options.</li> <li>The oscillator frequency or the external clock frequency must not exceed 4330 kHz</li> </ul>

#### [Caution]

The oscillator and divider options are summarized in the following tables. The information presented in those tables is crucial when using these products.

## Divider Options for the LC651204N/1202N, LC651204F/1202F and LC651204L/1202L

#### LC651204N/1202N

Circuit type	Frequency	Divider option (cycle time)	VDD range	Notes
Ceramic oscillator	800kHz	1/1 (5µs)	3 to 5.5V	
	1MHz	1/1 (4µs)	3 to 5.5V	
	4MHz	1/3 (3µs)	3 to 5.5V	This frequency cannot be used with the 1/1
		1/4 (4µs)	3 to 5.5V	divider (i.e., no divider circuit) option.
External clock generated by a	670k to 1444kHz	1/1 (6 to 2.77µs)	3 to 5.5V	
two-terminal RC oscillator circuit	2000k to 4330kHz	1/3 (6 to 2.77µs)	3 to 5.5V	
	2600k to 4330kHz	1/4 (6 to 3.70µs)	3 to 5.5V	
Use of external clock with the	Driving the circuit wit	h an external clock is not possible. To	use external c	lock drive, specify the two-terminal RC oscillator
ceramic oscillator option selected	option.			

#### LC651204F/1202F

Circuit type	Frequency	Divider option (cycle time)	VDD range	Notes
Ceramic oscillator	4MHz	1/1 (1µs)	3 to 5.5V	
External clock generated by a	670k to 4330kHz	1/1 (6 to 0.92µs)	3 to 5.5V	
two-terminal RC oscillator circuit				
Use of external clock with the	Driving the circuit wit	h an external clock is not possible. To	o use external cl	lock drive, specify the two-terminal RC oscillator
ceramic oscillator option selected	option.			

#### LC651204L/1202L

Circuit type	Frequency	Divider option (cycle time)	VDD range	Notes
Ceramic oscillator	800kHz	1/1 (5µs)	2.5 to 5.5V	
	1MHz	1/1 (4µs)	2.5 to 5.5V	
	4MHz	1/4 (4µs)	2.5 to 5.5V	This frequency cannot be used with the $1/1$ , $1/3$
				divider (i.e., no divider circuit) option.
External clock generated by a	670k to 1040kHz	1/1 (6 to 3.84µs)	2.5 to 5.5V	
two-terminal RC oscillator circuit	2000k to 3120kHz	1/3 (6 to 3.84µs)	2.5 to 5.5V	
	2600k to 4160kHz	1/4 (6 to 3.84µs)	2.5 to 5.5V	
Use of external clock with the	Driving the circuit wit	h an external clock is not possible. T	o use external c	lock drive, specify the two-terminal RC oscillator
ceramic oscillator option selected	option.			

## Port C and D Output State at Reset Options

The output levels at reset of the I/O ports C and D can be selected form the following two options, which are specified in 4-bit units.

Option	Conditions and notes
High-level output at reset	Ports C and D in 4-bit units
Low-level output at reset	Ports C and D in 4-bit units

## Port Output Circuit Type Option

The output circuit types of the I/O ports can be selected form the following two options in bit units.

Option	Circuit	Conditions and notes
Open drain output		Ports A, C, D, E, F and G
Pull-up resistor output		

## Watchdog Timer Reset Option

Whether the PE1/WDR pin functions as the normal port PE1 or as the WDR watchdog timer reset pin can be selected as an option.

#### LC651204N, LC651202N Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Applicable pins/notes	Conditions	Ratings	unit
Maximum supply voltage	VDD max		VDD	-30 to +7.0	V
Output voltage	VO		OSC2	Voltages up to any generated voltage are allowed.	
Input voltage	VI (1)		OSC1 *1	-0.3 to VDD +0.3	
	VI (2)		TEST, RES	-0.3 to VDD +0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to VDD +0.3	
	VIO (3)	PA0 to 3, PG0 to 3		-0.3 to VDD +0.3	
Peak output current	IOP		I/O ports	-2 to +20	mA
Average output current	IOA	Average value per pin over a 100-ms period	I/O ports	-2 to +20	
	$\Sigma IOA(1)$	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1*2	PC0 to PC3 PD0 to PD3 PE0 to PE1	-15 to +100	
	ΣIOA (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to PF3 PG0 to PG3 PA0 to PA3	-15 to +100	
Allowable power dissipation	Pd max(1)	$Ta = -40$ to $+85^{\circ}C$ (DIP package)		250	mW
	Pd max(2)	$Ta = -40$ to $+85^{\circ}C$ (MFP package)		150	
Operation temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	

#### Allowable Operating Range at Ta=-40°C to +85°C, VSS=0V, VDD=3.5 to 5.5V

(unless otherwise specified)

				(unicoo (			mou)
Parameter	Symbol	Conditions	Applicable pins/potes		unit		
r ai ainetei	Symbol	Conditions	Applicable phis/libles	min.	typ.	max.	um
Operating power-Supply voltage	VDD		VDD	3.0		5.5	V
Standby power-Supply voltage	VST	RAM and register values retained *3	VDD	1.8		5.5	
Input high-level voltage	VIH(1)	Output n-channel transistors off	OD specification ports C, D, E, and F	0.7VDD		13.5	
	VIH(2)	Output n-channel transistors off	PU specification ports C, D, E, and F	0.7VDD		VDD	
	VIH(3)	Output n-channel transistors off	Port A, G	0.7VDD		VDD	
	VIH(4)	Output n-channel transistors off	The $\overline{INT}$ , $\overline{SCK}$ , and SI pins with OD specifications	0.8VDD		13.5	
	VIH(5)	Output n-channel transistors off	The $\overline{INT}$ , $\overline{SCK}$ , and SI pins with PU specifications	0.8VDD		VDD	]
	VIH(6)	VDD = 1.8 to $5.5V$	RES	0.8VDD		VDD	
	VIH(7)	External clock specifications	OSC1	0.8VDD		VDD	

Demonstration	Grouphal	Conditions		Applicable		Ratings		unit
Parameter	Symbol	Conditions	Conditions			typ.	max.	unit
Input low-level	VIL(1)	Output n-channel transistors off	VDD = 4  to  5.5V	Port	VSS		0.2VDD	V
voltage	VIL(2)	Output n-channel transistors off	VDD = 3  to  5.5V	Port	VSS		0.2VDD	
	VIL(3)	Output n-channel transistors off	VDD = 4  to  5.5V	$\overline{INT}$ , $\overline{SCK}$ ,SI	VSS		0.2VDD	
	VIL(4)	Output n-channel transistors off	VDD = 3 to 5.5V	INT, SCK, SI	VSS		0.2VDD	
	VIL(5)	External clock specifications	VDD = 4  to  5.5V	OSC1	VSS		0.2VDD	
	VIL(6)	External clock specifications	VDD = 3  to  5.5V	OSC1	VSS		0.2VDD	
	VIL(7)		VDD = 4  to  5.5V	TEST	VSS		0.2VDD	
	VIL(8)		VDD = 3  to  5.5V	TEST	VSS		0.2VDD	
	VIL(9)		VDD = 4  to  5.5V	RES	VSS		0.2VDD	
	VIL(10)		VDD = 3 to 5.5V	RES	VSS		0.2VDD	
Operating frequency (cycle time)	fop (Tcyc)	Frequencies up to 4.33MHz are supported if the divide-by-three or divide-by-four divider circuit option is used.	VDD = 3 to 5.5V		670 (6)		1444 (2.77)	kHz (µs)
External clock conditions	text	Figure 1. The divide-by-three or divide-by-four divider circuit option must be used if the clock frequency.	VDD = 3 to 5.5V	OSC1	670		4330	kHz
Pulse width Rise and fall	textH, textL	exceeds 1.444MHz.	VDD = 3 to 5.5V	OSC1	69			ns
times	textR, textF		VDD = 3 to 5.5V	OSC1			50	
Guaranteed oscillator constants Ceramic oscillator		Figure 2				See Table 1.		

				(	unless o	therwise	e specif	ied)
Doror	notor	Symbol	Conditions	Applicable ping/potes		Ratings		unit
r ai ai	lietei	Symbol	Conditions	Applicable plins/libles	min.	typ.	max.	umi
Input high-le	evel	IIH(1)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= 13.5V	Ports C, D, E, and F with open-drain specifications			5.0	μA
		IIH(2)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= VDD	Ports A and G with open-drain specifications			1.0	
		IIH(3)	External clock mode, VIN= VDD	OSC1			1.0	
Input low-le	evel current	IIL(1)	Output n-channel transistors off VIN= VSS	Ports with open-drain specifications	-1.0			
		IIL(2)	Output n-channel transistors off VIN= VSS	Ports with pull-up resistor specifications	-1.3	-0.35		mA
		IIL(3)	VIN= VSS	RES	-45	-10		μΑ
		IIL(4)	External clock mode, VIN= VSS	OSC1	-1.0			
Output high-level voltage		VOH(1)	IOH= -50µA VDD= 4.0 to 5.5V	Ports with pull-up resistor specifications	VDD-1.2			v
		VOH(2)	IOH= -10µA VDD= 3.0 to 5.5V	Ports with pull-up resistor specifications	VDD-0.5			
Output low- voltage	level	VOL(1)	IOL= 10mA VDD= 4.0 to 5.5V	Port			1.5	
-		VOL(2)	IOL= 1 mA, with the IOL for all ports no more than 1 mA. VDD= 3.0 to 5.5V	Port			0.5	
Hyster	esis voltage	VHIS		$\overline{\text{RES}}$ , $\overline{\text{INT}}$ , $\overline{\text{SCK}}$ and $\overline{\text{SI}}$		0.1VDD		
High-le thresho	evel old voltage	VtH		specifications *4	0.4VDD		0.8VDD	
Low-le	evel old voltage	VtL			0.2VDD		0.6VDD	
Current drain	1	IDDOP(1)	Operating, output n-channel transistors off, Ports = VDD Figure 2, 4 MHz, divide-by-three circuit	VDD		1.5	5	mA
Ceramic osci	llator	IDDOP(2)	Figure 2, 4 MHz, divide-by-four circuit	VDD		1.5	4	
		IDDOP(3)	Figure 2, 800 kHz	VDD		1.5	4	
External cloc Standby mod	ik le	IDDOP(4)	670 to 1444 kHz, no divider circuit 2000 to 4330 kHz, divide-by-three circuit 2600 to 4330 kHz, divide-by-four circuit	VDD		1.5	5	
		IDDst	Output n-channel transistors off, $VDD = 5.5V$	VDD		0.05	10	μA
			Ports = VDD, $VDD = 3V$	VDD		0.025	5	•

## Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=3.0 to 5.5V

Deremator	Symbol	Conditions	Applicable pipe/potes		unit		
r al allietei	Symbol	Conditions	OSC1_OSC2		typ.	max.	um
Oscillator characteristics	fCFOSC *5	Figure 2, fo = 800 kHz Figure 2, fo = 1 MHz	OSC1, OSC2	768	800	832	kHz
Ceramic oscillator		Figure 2, fo = 4 MHz, divide-by-three or $divide by$ four circuit	OSC1, OSC2	960	1000	1040	
Oscillator stabilization time			OSC1, OSC2	3840	4000	1460	
stabilization time	tCFS	Figure 3, fo = 800 kHz, 1 MHz, 4 MHz Divide-by-three or divide-by-four circuit				5	ms
Pull-up resistors I/O ports	Rpp	Output n-channel transistors off VIN = VSS, VDD = 5V	Ports with pull-up resistor specifications	8	14	30	kΩ
RES	Ru	VIN = VSS, VDD = 5V	RES	100	250	400	
External reset characteristics Reset time	tRST				See Figure 4.		
Pin capacitance	Ср	f = 1MHz With all pins other than the pin being measured at VIN = VSS			10		pF
Serial clock	tCKCY(1)	Figure 5	SCK	3.0			μs
Input clock cycle time	tCKCY(2)	Figure 5	SCK		64×Tcyc *6		
Output clock cycle	tCKL(1)	Figure 5	SCK	1.0			
Input clock low-level	tCKL(2)	Figure 5	SCK		32×Tcyc		
pulse width	tCKH(1)	Figure 5	SCK	1.0			
Output clock low-level pulse width Input clock high-level pulse width Output clock high-level pulse width	tCKH(2)	Figure 5	SCK		32×Tcyc		

	Donomotor	Crumb al	Conditions		Applicable		Ratings		
	Parameter	Symbol	Conditions	VDD[V]	pins/notes	min.	typ.	max.	umit
Seria Data	al input a setup time	tICK	Stipulated with respect to the rising edge of $\overline{\text{SCK}}$ .		SI	0.4			μs
Data	hold time	tCKI	Figure 5		SI	0.4			
Seria Outț	al output out delay time	tCKO	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$		SO			0.6	
Puls Perio High	e output od wlevel pulse width	tPCY tPH	Figure 6 TCYC = $4 \times$ the system clock period For n-channel open-drain outputs only:		PE0 PE0		64×Tcyc 32×Tcyc		-
Low	-level pulse width		External resistance: $1 \text{ k}\Omega$ . external		110		± 10%		
	F	tPL	capacitance: 50 pF		PE0		32×TCYC ± 10%		
	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.1±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
I		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
ime	Clear time (discharge)	tWCT	See Figure 7.		WDR	100			μs
og t	Clear period (charge)	tWCCY	See Figure 7.		WDR	29			ms
'atchde	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	4 to 5.5	WDR		0.047±5%		μF
Wa		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	40			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	15			ms

[Notes]

- 1. When driven internally using the oscillator circuit shown in Figure 3 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.
- 2. The average over a 100-ms period
- 3. The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
- 4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
- 5. The values shown for fCFOSC are the frequencies for which oscillation is possible. The center frequency when a ceramic oscillator is used may differ by about 1% from the nominal value listed by the manufacturer of the ceramic oscillator element. See the specifications of the ceramic oscillator element for details.
- 6. TCYC =  $4 \times$  the system clock period
- 7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.



Figure 1 External Clock Input Waveform



Figure 2 Ceramic Oscillator Circuit





Table 1 : Guaranteed Ceramic Oscillator Constants

4MHz (Murata Mfg. Co., Ltd.)	C1	33 pF±10 %
CSA4.00MG	C2	33 pF±10 %
CST4.00MGW (built-in capacitor version)	R	$0\Omega$
4MHZ (Kyocera Corporation)	C1	33 pF±10 %
KBR4.0MSA	C2	33 pF±10 %
KBR4.0MKS (built-in capacitor version)	R	$0\Omega$
1MHz (Murata Mfg. Co., Ltd.)	C1	100 pF±10 %
CSB1000J	C2	100 pF±10 %
	R	2.2 kΩ
1MHz (Kyocera Corporation)	C1	100 pF±10 %
KBR1000F	C2	100p F±10 %
	R	$0\Omega$
800kHz (Murata Mfg. Co., Ltd.)	C1	100 pF±10 %
CSB800J	C2	100 pF±10 %
	R	2.2 kΩ
800kHz (Kyocera Corporation)	C1	220 pF±10 %
KBR800F	C2	220 pF±10 %
	R	$\Omega\Omega$



Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES =  $0.1 \ \mu F$  will be between 5 and 50 ms.

If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.



Figure 5 Serial I/O Timing







TWCCY : Charge time due to the external components Cw, Rw and Rl. TWCT : Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

#### LC651204F, LC651202F Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Applicable pins/notes	Conditions	Ratings	unit
Maximum supply voltage	VDD max		VDD	-30 to +7.0	v
Output voltage	VO		OSC2	Voltages up to any	
				generated voltage	
				are allowed.	
Input voltage	VI (1)		OSC1 *1	-0.3 to VDD +0.3	
	VI (2)		TEST, $\overline{\text{RES}}$	-0.3 to VDD +0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to VDD +0.3	
	VIO(3)	PA0 to 3, PG0 to 3		-0.3 to VDD +0.3	
Peak output current	IOP		I/O ports	-2 to +20	mA
Average output current	IOA	Average value per pin over a 100-ms period	I/O ports	-2 to +20	
	$\Sigma$ IOA (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0	PC0 to 3	-15 to +100	
		to 1*2	PD0 to 3		
			PE0 to 1		
	$\Sigma$ IOA (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0	PF0 to 3	-15 to +100	
		to 3*2	PG0 to 3		
			PA0 to 3		
Allowable power dissipation	Pd max(1)	$Ta = -40$ to $+85^{\circ}C$ (DIP package)		250	mW
	Pd max(2)	$Ta = -40$ to $+85^{\circ}C$ (MFP package)		150	
Operation temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	

## Allowable Operating Range at Ta=-40°C to +85°C, VSS=0V, VDD=3.0 to 5.5V

·	Ũ		(L	nless oth	erwis	se specifi	ied)
Denemator	Symphol	Conditions	Ampliashla mina/astas	]	<u></u> s		
Parameter	Symbol	Conditions	Applicable plits/hotes	min.	typ.	max.	umit
Operating	VDD		VDD	3.0		5.5	v
power-Supply voltage							
Standby	VST	RAM and register values retained *3	VDD	1.8		5.5	
power-Supply voltage							
Input high-level	VIH(1)	Output n-channel transistors off	OD specification ports C, D, E and F	0.7VDD		13.5	
voltage	VIH(2)	Output n-channel transistors off	PU specification ports C, D, E and F	0.7VDD		VDD	
	VIH(3)	Output n-channel transistors off	Port A, G	0.7VDD		VDD	
	VIH(4)	Output n-channel transistors off	The $\overline{INT}$ , $\overline{SCK}$ and SI pins with OD	0.8VDD		13.5	
			specifications				
	VIH(5)	Output n-channel transistors off	The $\overline{INT}$ , $\overline{SCK}$ and SI pins with PU	0.8VDD		VDD	
			specifications				
	VIH(6)	VDD = 1.8 to 5.5V	RES	0.8VDD		VDD	
	VIH(7)	External clock specifications	OSC1	0.8VDD		VDD	
Input low-level	VIL(1)	Output n-channel transistors off	Port	VSS		0.2VDD	
voltage	VIL(2)	Output n-channel transistors off	$\overline{INT}$ , $\overline{SCK}$ , SI	VSS		0.2VDD	
	VIL(3)	External clock specifications	OSC1	VSS		0.2VDD	
	VIL(4)		TEST	VSS		0.2VDD	
	VIL(5)		RES	VSS		0.2VDD	

		Continued from	n preceding page.				
Parameter	Symbol	Conditions	Applicable pins/notes	l	unit		
1 arameter	Symbol	Conditions	Applicable phils/libites	min.	typ.	max.	um
Operating frequency (cycle time) External clock conditions Frequency Pulse width Rise and fall times	fop (Tcyc) text textH, textL textR, textF	Figure 1	OSC1 OSC1 OSC1	670 (6) 670 69		4330 (0.97) 4330 50	kHz (µs) kHz ns
Guaranteed oscillator constants Ceramic oscillator		Figure 2			See Tal	ole 1.	

## Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=3.0 to 5.5V

				(unless	otherwi	se spec	ified)
Deremator	Symbol	Conditions	Applicable			unit	
r al allietel	Symbol	Conditions	pins/notes	min.	typ.	max.	unit
Input high-level	IIH(1)	Output n-channel transistors off	Ports C, D, E and F			5.0	μΑ
current		(Includes the n-channel transistors off leakage current.)	with open-drain				
		VIN= 13.5V	specifications				
	IIH(2)	Output n-channel transistors off	Ports A and G with			1.0	
		(Includes the n-channel transistors off leakage current.)	open-drain				
		VIN= VDD	specifications				
	IIH(3)	External clock mode, VIN= VDD	OSC1			1.0	
Input low-level	IIL(1)	Output n-channel transistors off	Ports with open-drain	-1.0			
current		VIN= VSS	specifications				
	IIL(2)	Output n-channel transistors off	Ports with pull-up	-1.3	-0.35		mA
		VIN= VSS	resistor specifications				
	IIL(3)	VIN= VSS	RES	-45	-10		μΑ
	IIL(4)	External clock mode, VIN= VSS	OSC1	-1.0			
Output high-level	VOH(1)	$IOH = -50\mu A$	Ports with pull-up	VDD-1.2			V
voltage			resistor specifications				
-	VOH(2)	$IOH = -10 \mu A$	Ports with pull-up	VDD-0.5			
			resistor specifications				
Output low-level	VOL(1)	IOL=10mA	Port			1.5	
voltage							
	VOL(2)	IOL=1mA, with the IOL for all ports no more than 1mA.	Port			0.5	

## LC651204N/F/L,LC651202N/F/L

			Continued fr	rom preceding	g page.				•
Parameter		Symbol	Conditions		Applicable pins/notes		Ratings	. <u> </u>	unit
	i urumeter	byinoor	Conditions		rippileuble pills/lious	min.	typ.	max.	unit
istics	Hysteresis voltage	VHIS			$\overline{\text{RES}}$ , $\overline{\text{INT}}$ , $\overline{\text{SCK}}$ and $\overline{\text{SI}}$		0.1VDD		v
aracter	High-level threshold	VtH	]		specifications *4	0.4VDD		0.8VDD	
nmitt ch	Low-level threshold	VtL	-			0.25VDD		0.6VDD	
Scł	voltage								
Curro Cera	ent drain mic oscillator	IDDOP(1)	Figure 2, 4 MHz 670 to 1444 kHz		VDD		2	6	mA
Exter	rnal clock	IDDOP(2)	*1 Operating, output n-channel transistors off, Ports = VDD		VDD		2	6	
Stan	dby mode	IDDst	Output n-channel transistors off,	VDD = 5.5V	VDD		0.05	10	μA
			Ports = VDD	VDD = 3V	VDD		0.025	5	
Oscillator characteristics Ceramic oscillator Oscillator frequency		fCFOSC	Figure 2, fo = 4 MHz *5		OSC1, OSC2	3840	4000	1460	kHz
Oscil time	llator stabilization	tCFS	Figure 3, fo = 4 MHz					5	ms
Pull- ports	up resistors I/O	Rpp	Output n-channel transistors off VIN = VSS, VDD = 5V		Ports with pull-up resistor specifications	8	14	30	kΩ
RES		Ru	VIN = VSS, VDD = 5V		RES	100	250	400	
Exter chara Rese	rnal reset acteristics t time	tRST					See Figure 4.		
Pin c	apacitance	Ср	f = 1MHz With all pins other than the pin beir VIN = VSS	ng measured at			10		pF
Seria Inpu	ll clock t clock cycle time	tCKCY(1)	Figure 5		SCK	2.0			μs
Outp time Inpu	ut clock cycle t clock low-level	tCKCY(2)	Figure 5		SCK		64×Tcyc *6		
pulse Outp pulse	e width out clock low-level e width	tCKL(1)	Figure 5		SCK	0.6			
Input pulse Outp high	clock high-level width out clock -level pulse width	tCKL(2)	Figure 5		SCK		32×Tcyc		
		tCKH(1)	Figure 5		SCK	0.6			
		tCKH(2)	Figure 5		SCK		32×Tcyc	<u> </u>	1

	Donomotor	Crumb al	Conditions		Applicable		Ratings		
	Parameter	Symbol	Conditions	VDD[V]	pins/notes	min.	typ.	max.	unit
Seri Data	al input 1 setup time	tICK	Stipulated with respect to the rising edge of $\overline{\text{SCK}}$ .		SI	0.2			μs
Data	hold time	tCKI	Figure 5		SI	0.2			
Seri Out	al output out delay time	tCKO	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$		SO			0.4	
Puls Peri Higi	e output od a-level pulse width	tPCY tPH	Figure 6 TCYC = $4 \times$ the system clock period For n-channel open-drain outputs only.		PE0 PE0		64×Tcyc 32×Tcyc		-
Low	-level pulse width		External resistance: 1 k $\Omega$ , external		120		± 10%		
	F	tPL	capacitance: 50 pF		PE0		32×TCYC ± 10%		
	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.01±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
r		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
ime	Clear time (discharge)	tWCT	See Figure 7.		WDR	10			μs
og t	Clear period (charge)	tWCCY	See Figure 7.		WDR	3.0			ms
'atchde	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	4.5 to 5.5	WDR		0.01±5%		μF
W		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	10			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	3.3			ms

[Notes]

- 1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.
- 2. The average over a 100-ms period
- 3. The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
- 4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
- 5. The values shown for fCFOSC are the frequencies for which oscillation is possible.
- 6. TCYC =  $4 \times$  the system clock period
- 7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.



Figure 1 External Clock Input Waveform



Figure 2 Ceramic Oscillator Circuit





Table 1 : Guaranteed Ceramic Oscillator Constants

4MHz (Murata Mfg. Co., Ltd.)	C1	33 pF±10 %
CSA4.00MG	C2	33 pF±10 %
CST4.00MGW (built-in capacitor version)	R	$\Omega \Omega$
4MHZ (Kyocera Corporation)	C1	33p F±10 %
	00	22 E 10.0/
KBR4.0MSA	$ C_2 $	33p F±10 %



Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1μF will be between 5 and 50 ms.If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.



Figure 5 Serial I/O Timing



With load conditions identical to those shown in Figure 5

Figure 6 Port PE0 Pulse Output Timing



TWCCY : Charge time due to the external components Cw, Rw and Rl. TWCT : Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

#### LC651204L, LC651202L Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Applicable pins/notes	Conditions	Ratings	unit
Maximum supply voltage	VDD max		VDD	-30 to +7.0	V
Output voltage	VO		OSC2	Voltages up to any generated voltage are	
				allowed.	
Input voltage	VI (1)		OSC1 *1	-0.3 to VDD +0.3	
	VI (2)		TEST, RES	-0.3 to VDD +0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to VDD +0.3	
	VIO (3)	PA0 to 3, PG0 to 3		-0.3 to VDD +0.3	
Peak output current	IOP		I/O ports	-2 to +20	mA
Average output current	IOA	Average value per pin over a 100-ms period	I/O ports	-2 to +20	
	$\Sigma$ IOA (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0	PC0 to 3	-15 to +100	
		to 1*2	PD0 to 3		
			PE0 to 1		
	$\Sigma$ IOA (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0	PF0 to 3	-15 to +100	
		to 3*2	PG0 to 3		
			PA0 to 3		
Allowable power dissipation	Pd max(1)	$Ta = -40$ to $+85^{\circ}C$ (DIP package)		250	mW
	Pd max(2)	$Ta = -40$ to $+85^{\circ}C$ (MFP package)		150	
Operation temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	

#### Allowable Operating Range at Ta=-40°C to +85°C, VSS=0V, VDD=2.5 to 5.5V

#### (unless otherwise specified) Ratings Applicable pins/notes Parameter Symbol Conditions unit typ. max. min. VDD VDD Operating 2.5 5.5 V power-Supply voltage RAM and register values retained \*3 VDD Standby VST 1.8 5.5 power-Supply voltage OD specification ports C, D, E and F PU specification ports C, D, E and F Input high-level VIH(1) 0.7VDD Output n-channel transistors off 13.5 voltage VIH(2) Output n-channel transistors off 0.7VDD VDD VIH(3) Output n-channel transistors off Port A, G 0.7VDD VDD VIH(4) Output n-channel transistors off The $\overline{INT}$ , $\overline{SCK}$ and SI pins with OD 0.8VDD 13.5 specifications VIH(5) Output n-channel transistors off 0.8VDD VDD The $\overline{INT}$ , $\overline{SCK}$ and SI pins with PU specifications VIH(6) VDD = 1.8 to 5.5 V0.8VDD VDD RES VIH(7)0.8VDD VDD External clock specifications OSC1 0.2VDD Input low-level VIL(1) VSS Output n-channel transistors off Port voltage 0.15VDD VIL(2) Output n-channel transistors off VSS INT, SCK ,SI VIL(3) External clock specifications OSC1 VSS 0.15VDD 0.2VDD VIL(4) TEST VSS VIL(5) VSS 0.15VDD RES

Donomoton	Sample of	Conditions	Applicable size/setes	I	Ratings		
Parameter	Symbol	Conditions	Applicable plus/liotes	min.	typ.	max.	um
Operating		Frequencies up to 4.16MHz are supported					
frequency	fop	if the divide-by-four divider circuit option		670		1040	kHz
(cycle time)	(Tcyc)	is used.		(6)		(3.84)	(µs)
External clock		Figure 1. The divide-by-three or					
conditions	text	divide-by-four divider circuit option	OSC1	670		4160	kHz
Frequency		must be used if the clock frequency					
Pulse width	textH,	exceeds 1.040MHz.	OSC1	150			ns
Rise and fall times	textL						
	textR,		OSC1			100	
	textF						
Guaranteed		Figure 2			See Tal	ole 1.	
oscillator							
constants							
Ceramic oscillator							

## Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=2.5 to 5.5V

		, , ,					
				(unless	otherwi	se speci	ified)
Doromotor	Symbol	Conditions	(unless otherwise specified)ConditionsApplicable pins/notesRatings min.unitnsistors off nel transistors off leakage current.)Ports C, D, E and F with open-drain specifications5.0µAnsistors off nel transistors off leakage current.)Ports A and G with open-drain specifications1.01.0VIN= VDD nsistors offOSC1 Ports with open-drain specifications1.01.0nsistors off nsistors offPorts with open-drain specifications-1.3-0.35mAVIN= VDD nsistors offPorts with pull-up resistor specifications-45-10µAVIN= VSSOSC1 resistor specifications-1.0VINVDD-0.5VPorts with pull-up resistor specifications-1.01.5V				
Parameter	Symbol	Collditions	pins/notes	min.	typ.	max.	um
Input high-level	IIH(1)	Output n-channel transistors off	Ports C, D, E and F			5.0	μA
current		(Includes the n-channel transistors off leakage current.)	with open-drain				
		VIN= 13.5V	specifications				
	IIH(2)	Output n-channel transistors off	Ports A and G with	1		1.0	
		(Includes the n-channel transistors off leakage current.)	open-drain	1			
		VIN= VDD	specifications				
	IIH(3)	External clock mode, VIN= VDD	OSC1			1.0	
Input low-level	IIL(1)	Output n-channel transistors off	Ports with open-drain	-1.0			
current		VIN= VSS	specifications	1			
	IIL(2)	Output n-channel transistors off	Ports with pull-up	-1.3	-0.35		mA
		VIN= VSS	resistor specifications	1			
	IIL(3)	VIN= VSS	RES	-45	-10		μΑ
	IIL(4)	External clock mode, VIN= VSS	OSC1	-1.0			1
Output high-level	VOH(1)	IOH= -10µA	Ports with pull-up	VDD-0.5			V
voltage			resistor specifications				
Output low-level	VOL(1)	IOL= 3mA	Port			1.5	1
voltage				1			
	VOL(2)	IOL= 1 mA, with the IOL for all ports no more than	Port			0.4	1
		1 mA.					

Daramatar	Symbol	Conditions		Applicable ning/notes		-	unit	
	Symbol	Conditions		Applicable phils/libles	min.	typ.	max.	um
Hysteresis voltage	VHIS			$\overline{\text{RES}}$ , $\overline{\text{INT}}$ , $\overline{\text{SCK}}$ and $\overline{\text{SI}}$		0.1VDD		v
High-level	VtH			oSC1 with schmitt specifications *4	0.4VDD		0.8VDD	
Low-level threshold voltage	VtL				0.2VDD		0.6VDD	
Current drain Ceramic oscillator	IDDOP(1)	Operating, output n-channel transistors Ports = VDD Figure 2, 4 MHz, divide-by-three circuit	off, it	VDD		1.5	4	mA
	IDDOP(2)	Figure 2, 4 MHz, divide-by-three circuit VDD = 2.5V	it	VDD		0.5	1	
	IDDOP(3)	Figure 2, 800 kHz		VDD		1.5	4.0	
External clock	IDDOP(4)	670 to 1024 kHz, no divider circuit 2000 to 3120 kHz, divide-by-three circ 2600 to 4160 kHz, divide-by-four circu	uit it	VDD		1.5	4	
Standby mode	IDDst	Output n-channel transistors off, Ports	VDD = 5.5V	VDD		0.05	10	μΑ
		= VDD	VDD = 2.5V	VDD		0.020	4	
Oscillator characteristics Ceramic oscillator	fCFOSC *5	Figure 2, fo = $800 \text{ kHz}$ Figure 2, fo = $1 \text{ MHz}$		OSC1, OSC2	768	800	832	kHz
Oscillator frequency Oscillator stabilization		Figure 2, fo = 4 MHz, divide-by-four ci	ircuit	OSC1, OSC2	960	1000	1040	
time				OSC1, OSC2	3840	4000	4160	
	tCFS	Figure 3, fo = 800 kHz, 1 MHz divide-by-four circuit	z, 4 MHz,				5	ms
Pull-up resistors I/O ports	Rpp	Output n-channel transistors off $VIN = VSS$ , $VDD = 5V$		Ports with pull-up resistor specifications	8	14	30	kΩ
RES	Ru	VIN = VSS, VDD = 5V		RES	100	250	400	
External reset characteristics Reset time	tRST				See Figure 4.			
Pin capacitance	Ср	f = 1MHz With all pins other than the pin being VIN = VSS	measured at			10		pF
Serial clock Input clock cycle time	tCKCY(1)	Figure 5		SCK	6.0			μs
Output clock cycle time Input clock low-level pulse width	tCKCY(2)	Figure 5		SCK		64×Tcyc *6		
Output clock low-level pulse width Input clock high-level	tCKL(1)	Figure 5		SCK	2.0			
pulse width Output clock high-level pulse width	tCKL(2)	Figure 5		SCK		32×Tcyc		
	tCKH(1)	Figure 5		SCK	2.0			
	tCKH(2)	Figure 5		SCK		32×Tcyc		

	Doromotor	Symbol	Conditions		Applicable		Ratings		unit
	Farameter	Symbol	Conditions	VDD[V]	pins/notes	min.	typ.	max.	um
Seri	al input		Stipulated with respect to the rising edge		SI	0.5			μs
Data	a setup time	tICK	of SCK .						
Data	a hold time	tCKI	Figure 5		SI	0.5			
Seri	al output	tCKO	Stipulated with respect to the rising edge		SO			1.0	
Out	put delay time		of $\overline{\text{SCK}}$ .						
			For n-channel open-drain outputs only:						
			External resistance: 1 k $\Omega$ , external						
			capacitance: 50 pF						
<b>D</b> 1			Figure 5						
Puls	e output period	tPCY	Tage $= 4 \times \text{the system clock period}$		PE0		64×TCYC		
Hig	h-level pulse width	tPH	For n-channel open-drain outputs only:		PE0		32×TCYC		
	i level puble viluit		External resistance: 1 k $\Omega$ , external				± 10%		_
Low	-level pulse width	tPL	capacitance: 50 pF		PE0		32×TCYC ± 10%		
	Guaranteed constants *7	CW	When PE1 has open-drain output	2.5 to 5.5	WDR		0.1±5%		μF
			specifications						· ·
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output		WDR		100±1%		Ω
er			specifications						
tim	Clear time (discharge)	tWCT	See Figure 7.		WDR	100			μs
00	Clear period (charge)	tWCCY	See Figure 7.		WDR	26			ms
atchd	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	2.5 to 5.5	WDR		0.047±5%		μF
A		RW	When PE1 has open-drain output		WDR		680±1%		kΩ
			specifications						
		RI	When PE1 has open-drain output		WDR		100±1%		Ω
		AVICT	specifications		WDD	40			
	Clear time (discharge)	twer	See Figure 7.		WDR	40			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	12			ms

[Notes]

- 1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.
- 2. The average over a 100-ms period
- 3. The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
- 4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
- 5. The values shown for fCFOSC are the frequencies for which oscillation is possible.
- 6. TCYC =  $4 \times$  the system clock period
- 7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.



Figure 1 External Clock Input Waveform



Figure 2 Ceramic Oscillator Circuit



Figure 3 Oscillator Stabilization Period

Table 1 : Guaranteed Cerar	nic Oscillator Constants
----------------------------	--------------------------

4MHz Murata Mfg. Co., Ltd.)	C1	33 pF±10 %
CSA4.00MGU	C2	33 pF±10 %
CST4.00MGWU (built-in capacitor version)	R	$\Omega \Omega$
1MHz (Murata Mfg. Co., Ltd.)	C1	100 pF±10 %
CSB1000J	C2	100 pF±10 %
	R	$2.2 \text{ k}\Omega$
1MHz (Kyocera Corporation)	C1	100 pF±10 %
KBR1000F	C2	100 pF±10 %
	R	$0\Omega$
800kHz (Murata Mfg. Co., Ltd.)	C1	100 pF±10 %
CSB800J	C2	100 pF±10 %
	R	$2.2 \mathrm{k}\Omega$
800kHz (Kyocera Corporation)	C1	220 pF±10 %
KBR800F	C2	220 pF±10 %
	R	$0\Omega$



Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES =  $0.1\mu$ F will be between 5 and 50 ms. If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.



Figure 5 Serial I/O Timing



Figure 6 Port PE0 Pulse Output Timing



TWCCY : Charge time due to the external components Cw, Rw and Rl. TWCT : Discharge time due to program processing

Figure 7 Watchdog Timer Waveform

## LC651204/1202 Instruction Set (by function) Abbreviations

AC	:	Accumulator	М	:	Memory	ZF	:	Zero flag
ACt	:	Accumulator bit t	M(DP)	:	Memory addressed by DP	0[]	:	Indicates the contents of
CF	:	Carry flag	P(DPL)	:	I/O port specified by DPL			the item enclosed.
CTL	:	Control register	PC	:	Program counter	$\leftarrow$	:	Transfer and direction
DP	:	Data pointer	STACK	:	Stack pointer	+	:	Addition
Е	:	E register	TM	:	Timer	-	:	Subtraction
EXTF	:	External interrupt request flag	TMF	:	Timer (internal) interrupt request flag	^	:	Logical AND
Fn	:	Flag bit n	At, Ha, La	:	Working registers	$\vee$	:	Logical OR
						$\forall$	:	Logical exclusive OR

group Number of bytes Number of bytes Modified Instruction code status nstruction Mnemonic Operation Description Notes flags D7 D6 D5 D4 D3 D2 D1 D0 1 1 0 Clears AC. CLA Clear AC 0 0 0 0 1 1  $AC \leftarrow 0$ ZF \*1 Accumulator manipulation instruction Clear CF 1 1 0 0 0 1  $CF \leftarrow 0$ Clears CF. CF CIC 1 1 1 1 0 Sets CF STC Set CF 1 1  $CF \leftarrow 1$ CF Sets AC to the one's CMA Complement AC 1 1 ZF  $AC \leftarrow (\overline{AC})$ 0 0 0 Increments AC INC Increment AC 1 1 1 0 1  $AC \leftarrow (AC) + 1$ ZF CF 1 DEC Decrement AC 0 0 0  $AC \leftarrow (AC) - 1$ Decrements AC. CF 1 1 1 1 ZF  $AC \leftarrow (CF), CA_{n+1} \leftarrow (AC_n), CF \leftarrow (AC_3)$ RAL Rotate AC left 0 Shifts AC together with CF ZF CF 0 0 0 0 1 1 left. through CF TAE Transfer AC to E 0 0 0 0 0 1  $E \leftarrow (AC)$ Moves the contents of AC 1 1 to E. XAE Exchange AC with E 0 0 0  $(AC) \leftrightarrow (E)$ Exchanges the contents of 0 1 1 AC and E. 0 0 1  $M(DP) \leftarrow [M(DP)] + 1$ Increments M(DP). INM Increment M 1 1 1 0 CF 1 1 ZF ory manipulatio 0 0 1 1 1 1  $M(DP) \leftarrow [M(DP)] - 1$ Decrements M(DP). DEm Decrement M CF 1 1 ZF instructions 0 0 0 0 B1 B  $M(DP, B_1 B_0) \leftarrow 1$ Sets the bit in M(DP) SmB bit Set M data bit 1 1 specified by B1 B0 to 1. 0 0 1 1 0 BiB Clears the bit in M(DP) RMB bit Reset M data bit 1 1  $M(DP, B_1 B_0) \leftarrow 0$ specified by B1 B0 to 0. Add M to AC AD 0 1 1 0 0 0 0 1 1  $AC \leftarrow (AC) + [M(DP)]$ Adds the contents of AC ZF CF and M(DP) as two's complement quantities and stores the result in AC. ADC Add M to AC with CF 0 0 1 0 0 0 0 1  $AC \leftarrow (AC) + [M(DP)]$ Adds the contents of AC, ZF CF 1 (CF) CF and M(DP) as two's complement quantities and stores the Arithmetic and comparison instructions result in AC. DAA Decimal adjust AC in 1 1 1 0 1 1 0 1 1  $AC \leftarrow (AC) + 3$ Adds 6 to AC. ZF addition Adds 10 to AC. DAS Decimal adjust AC in 0 1 1  $AC \leftarrow (AC) + 10$ ZF 1 1 ( subtraction EXL Exclusive or M to AC 0 1 0 1  $AC \leftarrow (AC) \forall [M(DP)]$ Takes the logical exclusive ZF 1 1 OR of AC and M(DP) and stores the result in AC. AND And M to AC 1 1 1 0 1 1 1 1  $AC \leftarrow (AC) \land [M(DP)]$ Takes the logical AND ZF of AC and M(DP) and stores the result in AC. OR Or M to AC 1 1 0 1 0  $AC \leftarrow (AC) \lor [M(DP)]$ Takes the logical OR of ZF 1 1 AC and M(DP) and store the result in AC. Compares the contents of ZF CF  $\overline{M(DP)}$ ] + (AC) + 1 AC and M(DP) and sets or clears CF and ZF CM Compare AC with M 1 1 1 1 0 1 1 1 1 accordingly.  $\begin{array}{c|c} Magnitude relationship & CF & ZF \\ \hline [M(DP)] > (AC) & 0 & 0 \\ \hline [M(DP)] = (AC) & 1 & 1 \\ \hline [M(DP)] < (AC) & 1 & 0 \end{array}$ 

Instruction group		Mnemonic	Instruct	D3 D2 D1 D0	Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
etic and comparison instructions	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	2	2	$\overline{\mathrm{I}_3\mathrm{I}_2\mathrm{I}_1\mathrm{I}_0} + (\mathrm{AC}) + 1$	Compares the contents of AC and the immediate data Is I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> and sets or clears CF and ZF accordingly. Magnitude relationship CFI ZF is I <sub>2</sub> I <sub>0</sub> $\sim$ (AC) 0 0 Is I <sub>2</sub> I <sub>1</sub> $\sim$ (AC) 1 1 I <sub>3</sub> I <sub>1</sub> $\mid$ $\mid$ $\sim$ (AC) 1 0	ZF CF	
Arithme	CLI data	Compare DP <sub>L</sub> with immediate data	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	1 1 0 0 I3 I2 I1 I0	2	2	(DPL) V I3 I2 I1 I0	Compares the contents of DP <sub>L</sub> and the immediate data.	ZF	
	LI data	Load AC with immediate data	1 1 0 0	I3 I2 I1 I0	1	1	$AC \leftarrow I_3 I_2 I_1 I_0$	Loads AC with the immediate data I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0.</sub>	ZF	*1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	$M(DP) \leftarrow (AC)$	Stores the contents of AC at M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	$AC \leftarrow [M(DP)]$	Loads the contents of M(DP) into AC.	ZF	
ctions	XM data	Exchange AC with M then modify DP <sub>H</sub> with immediate data	1 0 1 0	0 M2 M1 M0	1	2	$\begin{array}{l} (AC) \leftrightarrow [M(DP)] \\ DP_{\text{H}} \leftarrow (DP_{\text{H}}) \ \forall \ 0 \ M_2 \ M_1 \\ M_0 \end{array}$	Exchanges the contents of AC and M(DP). Then, replaces the contents of DP <sub>H</sub> with (DP <sub>H</sub> ) $\forall 0 M_2$ M <sub>1</sub> M <sub>0</sub> .	ZF	ZF is set to indicate the result of the $(DP_H) \forall 0$ $M_2 M_1 M_0$ operation.
store instruc	Х	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	$(AC) \leftrightarrow [M(DP)]$	Exchanges the contents of AC and M(DP).	ZF	ZF is set according to the contents of DPH at the point the instruction was executed.
Load and	XI	Exchange AC with M then increment DPL	1 1 1 1	1 1 1 0	1	2	$\begin{array}{l} (AC) \leftrightarrow [M(DP)] \\ DP_L \leftarrow (DP_L) + 1 \end{array}$	Exchanges the contents of AC and M(DP). Then, increments the contents of $DP_L$	ZF	ZF is set to indicate the result of the DPL + 1 operation.
	XD	Exchange AC with M then increment DPL	1 1 1 1	1 1 1 1	1	2	$(AC) \leftrightarrow [M(DP)]$ $DP_L \leftarrow (DP_L) - 1$	Exchanges the contents of AC and M(DP). Then, Decrements the contents of DP <sub>L</sub> .	ZF	ZF is set to indicate the result of the DP <sub>L</sub> + 1 operation.
	RTBI	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, $E \leftrightarrow ROM$ (PCh, E, AC)	Loads into AC and E the ROM data stored at the location given by the lower 8 bits of the PC, E and AC.		
uctions	LDZ data	Load DP <sub>H</sub> with Zero and DP <sub>L</sub> with immediate data respectively	1 0 0 0	I3 I2 I1 I0	1	1	$\begin{array}{llllllllllllllllllllllllllllllllllll$	Loads 0 into $DP_{H}$ and the immediate data $I_3 I_2 I_1 I_0$ into $DP_{L}$ .		
instr	LHI data	Load DP <sub>H</sub> with immediate data	0 1 0 0	I3 I2 I1 I0	1	1	$DP_H \leftarrow I_3  I_2  I_1  I_0$	Loads the immediate data $I_3$ I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> into DP <sub>H</sub> .		
lation	IND	Increment DPL	1 1 1 0	1 1 1 0	1	1	$DP_L \leftarrow (DP_L) + 1$	Increments the contents of DPL.	ZF	
anipu	DED	Decrement DPL	1 1 1 0	1 1 1 1	1	1	$DP_L \leftarrow (DP_L) - 1$	Decrements the contents of DPL.	ZF	
iter m	TAL	Transfer AC to DPL	1 1 1 1	0 1 1 1	1	1	$DP_{L} \leftarrow (AC)$	Moves the contents of AC to DP <sub>L</sub> .		
a poir	TLA	Transfer DP <sub>L</sub> to AC	1 1 1 0	1 0 0 1	1	1	$AC \leftarrow (DP_L)$	Moves the contents of DPL to AC.	ZF	
Dat	ХАН	Exchange AC with DP <sub>H</sub>	0 0 1 0	0 0 1 1	1	1	$(AC) \leftrightarrow (DP_{H})$	Exchanges the contents of AC and DP <sub>H</sub> .		

ruction group		Mnemonic	Instruct	ion code	nber of bytes	nber of bytes	Operation	Description	Modified status flags	Notes
Inst			D7 D6 D5 D4	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	nu	ιnN				
lation instructions	XAt XA0 XA1 XA2 XA3	Exchange AC with working register At	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	1 1 1 1	1 1 1 1	$\begin{array}{l} (\mathrm{AC}) \leftrightarrow (\mathrm{A_0}) \\ (\mathrm{AC}) \leftrightarrow (\mathrm{A_1}) \\ (\mathrm{AC}) \leftrightarrow (\mathrm{A_2}) \\ (\mathrm{AC}) \leftrightarrow (\mathrm{A_2}) \\ (\mathrm{AC}) \leftrightarrow (\mathrm{A_3}) \end{array}$	Exchanges the contents of AC and the working register A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> or A <sub>3</sub> specified by t <sub>1</sub> t <sub>0</sub> .		
ister manipul	XHa XH0 XH1	Exchange DP <sub>H</sub> with working register Ha	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{smallmatrix} & a \\ 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 \end{smallmatrix}$	1 1	1 1	$\begin{array}{l} (\mathrm{DP}_{\mathrm{H}}) \leftrightarrow (\mathrm{H}_{0}) \\ (\mathrm{DP}_{\mathrm{H}}) \leftrightarrow (\mathrm{H}_{1}) \end{array}$	Exchanges the contents of DP <sub>H</sub> and the working register H <sub>0</sub> or H <sub>1</sub> specified by a.		
Working reg	XLa XL0 XL1	Exchange DP <sub>H</sub> with working register Ha	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$egin{array}{ccccccc} & a & & & \\ 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 \end{array}$	1 1	1 1	$\begin{array}{l} (\mathrm{DP}_{\mathrm{L}}) \leftrightarrow (\mathrm{L}_{0}) \\ (\mathrm{DP}_{\mathrm{L}}) \leftrightarrow (\mathrm{L}_{1}) \end{array}$	Exchanges the contents of $DP_L$ and the working register $L_0$ or $L_1$ specified by a.		
ation	SFB flag	Set flag bit	0 1 0 1	B3 B2 B1 B0	1	1	$Fn \leftarrow 1$	Sets the flag specified by $B_3$ , $B_2$ , $B_1$ , $B_0$ to 1		
Memory manipul instructions	RFB flag	Reset flag bit	0 0 0 1	B3 B2 B1 B0	1	1	Fn ← 0	Clears the flag specified by B <sub>3</sub> , B <sub>2</sub> , B <sub>1</sub> , B <sub>0</sub> to 0.	ZF	The flags are divided into four groups, F0 to F3, F4 to F7, F8 to F12 to F15. ZF is set or cleared according to the 4 bits included in the specified flags.
suc	JMP addr	Jumping in the current bank	0 1 1 0 P7 P6 P5 P4	1 P10 P9 P8 P3 P2 P1 P0	2	2	$\begin{array}{c} PC \leftarrow P_{10} \ P_{9} \ P_{8} \ P_{7} \ P_{6} \\ P_{5} \ P_{4} \ P_{3} \ P_{2} \ P_{1} \ P_{0} \end{array}$	Jumps to the location specified by the immediate data P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> .		
nstructio	JPEA	Jumping current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	PC0 to 7 $\leftarrow$ (E, AC)	Jumps to the location given by replacing the lower 8 bits of the PC with E and AC.		
routine ii	CZP addr	Call subroutine in the zero page	1 0 1 1	P3 P2 P1 P0	1	1	$\begin{aligned} \text{STACK} &\leftarrow (\text{PC}) + 1 \\ \text{PC10 to 6, PC1 to 0} &\leftarrow 0 \\ \text{PC5 to 2} &\leftarrow \text{P}_3 \text{P}_2 \text{P}_1 \text{P}_0 \end{aligned}$	Calls a subroutine on page 0.		
idus	CAL addr	Call subroutine	1 0 1 0	1 P10 P9 P8	2	2	$STACK \leftarrow (PC) + 2$	Calls a subroutine.		
s pu	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$	Returns from a subroutine.		
mp ai	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$ $CF, ZF \leftarrow CSF, ZSF$	Returns from an interrupt handling routine.	ZF CF	
Ju	BANK	Change bank	1 1 1 1	1 1 0 1	1	1		Specifies a pseudo I/O port and changes the bank.		Only valid for the immediately following JMP, I/O, or branch instruction.

Instruction group		Mnemonic	Instruct	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
	BAt addr	Change bank	P7 P6 P5 P4	P3 P2 P1 P0	2	2	$PC.7 \text{ to } 0 \leftarrow P_7 P_8 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $ACt = 1$	Branches to the location on the same page specified by $P_7$ to $P_0$ if the bit in AC specified by the immediate data $t_1$ to is 1.		BA0 to BA3, reflecting the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 P7 P6 P5 P4	0 0 ti to P3 P2 P1 P0	2	2	$\begin{array}{l} PC7 \text{ to } 0 \leftarrow P_7 \ P_6 \ P_5 \ P_4 \\ P_3 \ P_2 \ P_1 \ P_0 \end{array}$ if ACt = 0	Branches to the location on the same page specified by P7 to $P0$ if the bit in AC specified by the immediate data t <sub>1</sub> t <sub>0</sub> is 0.		The mnemonics are BNA0 to BNA3, reflecting the value of t.
	BMt addr	Branch on M bit	0 1 1 1 P7 P6 P5 P4	0 1 ti to P3 P2 P1 P0	2	2	$\begin{array}{l} PC7 \text{ to } 0 \leftarrow P7 \ P6 \ P5 \ P4 \\ P3 \ P2 \ P1 \ P0 \\ \text{ if } [M(DP, t_1 t_0)] = 1 \end{array}$	Branches to the location on the same page specified by P7 to P0 if the bit in $M(DP)$ specified by the immediate data tu to is 1.		The mnemonics are BM0 to BM3, reflecting the value of t.
SU	BNMt addr	Branch on no M bit	0 0 1 1 P7 P6 P5 P4	0 1 ti to P3 P2 P1 P0	2	2	$PC7 \text{ to } 0 \leftarrow P7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ $\text{if } [M(DP, t_1 t_0)] = 0$	Branches to the location on the same page specified by P7 to P0 if the bit in $M(DP)$ specified by the immediate data t1 to is 0.		The mnemonics are BNM0 to BNM3, reflecting the value of t.
ch instructio	BPt addr	Branch on Port bit	0 1 1 1 P7 P6 P5 P4	1 0 t <sub>1</sub> t <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	$PC7 \text{ to } 0 \leftarrow P7 P_6 P_5 P_4$ $P_3 P_2 P_1 P_0$ if $[P(DP_{L}, t_1 t_0)] = 1$	Branches to the location on the same page specified by P7 to P0 if the bit in $P(DP_L)$ specified by the immediate data tu to is 1.		The mnemonics are BP0 to BP3 , reflecting the value of t.
Bran	BNPt addr	Branch on no Port bit	0 0 1 1 P7 P6 P5 P4	1 0 ti to P3 P2 P1 P0	2	2	$PC7 \text{ to } 0 \leftarrow P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0 if [P(DP_{L}, t_1 t_0)] = 0$	Branches to the location on the same page specified by P7 to P0 if the bit in P(DPL) specified by the immediate data $t_1$ to is 0.		The mnemonics are BNP0 to BNP3 , reflecting the value of t.
	BTM addr	Branch on timer	0 1 1 1 P7 P6 P5 P4	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	2	2	$\begin{array}{c} PC7 \text{ to } 0 \leftarrow P_7 P_6 P_5 P_4 \\ P_7 P_6 P_5 P_4 \end{array}$ if TMF = 0 then TMF $\leftarrow 0$	Branches to the location on the same page specified by P7 to P0 if TMF is 1. Also clears TMF.	TMF	
	BNTM addr	Branch on no timer	0 0 1 1 P7 P6 P5 P4	1 1 0 0 P3 P2 P1 P0	2	2	$\begin{array}{c} PC7 \text{ to } 0 \leftarrow P7 P_6 P_5 P_4 \\ P7 P_6 P_5 P_4 \end{array}$ if TMF = 0 then TMF $\leftarrow 0$	Branches to the location on the same page specified by P7 to P0 if TMF is 0. Also clears TMF.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 P7 P6 P5 P4	1 1 0 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7 to $0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ if EXTF = 1 then EXTF $\leftarrow 0$	Branches to the location on the same page specified by P7 to P0 if EXTF is 1. Also clears EXTF.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 P7 P6 P5 P4	1 1 0 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	$PC7 \text{ to } 0 \leftarrow P_7 P_6 P_5 P_4$ $P_7 P_6 P_5 P_4$ $if EXTF = 0$ $then EXTF \leftarrow 0$	Branches to the location on the same page specified by P7 to P0 if EXTF is 0. Also clears EXTF.	EXTF	

Instruction group	Mnemonic		Instruction code D7 D6 D5 D4 D3 D2 D1 D0		Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
Branch instructions	BC addr	Branch on CF	0 1 1 1 P7 P6 P5 P4	1 1 1 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	$\begin{array}{c} PC7 \text{ to } 0 \leftarrow P_7 P_6 P_5 P_4 \\ P_7 P_6 P_5 P_4 \\ \text{if EXTF} = 0 \end{array}$	Branches to the location on the same page specified by P7 to P0 if CF is 1.		
	BNC addr	Branch on no CF	0 0 1 1 P7 P6 P5 P4	1 1 1 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	$\begin{array}{c} PC7 \text{ to } 0 \leftarrow P7 P6 P5 P4 \\ P7 P6 P5 P4 \\ \text{if } CF = 0 \end{array}$	Branches to the location on the same page specified by $P_7$ to $P_0$ if CF is 0.		
	BZ addr	Branch on ZF	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	2	2	$\begin{array}{c} PC7 \text{ to } 0 \leftarrow P_7 P_6 P_5 P_4 \\ P_7 P_6 P_5 P_4 \\ \text{if } ZF = 1 \end{array}$	Branches to the location on the same page specified by P7 to P0 if ZF is 1.		
	BNZ addr	Branch on no ZF	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	$\begin{array}{c} PC7 \text{ to } 0 \leftarrow P7 P_6 P_5 P_4 \\ P7 P_6 P_5 P_4 \\ \text{if } ZF = 0 \end{array}$	Branches to the location on the same page specified by P7 to P0 if ZF is 0.		
	BFn addr	Branch on flag bit	1 1 0 1 P7 P6 P5 P4	ns n2 n1 n0 P3 P2 P1 P0	2	2	$\begin{array}{l} PC7 \text{ to } 0 \leftarrow P_7 \ P_6 \ P_5 \ P_4 \\ P_7 \ P_6 \ P_5 \ P_4 \end{array}$ if Fn = 1	Branches to the location on the same page specified by P7 to P0 if the bit in the 16 flags specified by n3 n2 n1 n0 is 1.		The mnemonics are BF0 to BF15, reflecting the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 P7 P6 P5 P4	n3 n2 n1 n0 P3 P2 P1 P0	2	2	$ \begin{array}{l} PC7 \mbox{ to } 0 \leftarrow P_7 \mbox{ $P_6$ $P_5$ $P_4$} \\ P_7 \mbox{ $P_6$ $P_5$ $P_4$} \\ \mbox{ if $Fn=0$} \end{array} $	Branches to the location on the same page specified by P7 to P0 if the bit in the 16 flags specified by n3 n2 n1 n0 is 0.		The mnemonics are BFN0 to BFN15, reflecting the value of n.
I/O instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	$AC \leftarrow [P(DP_L)]$	Inputs the contents of port P(DP <sub>L</sub> ) to AC.	ZF	
	OP	Output port to AC	0 1 1 0	0 0 0 1	1	1	$P(DP_{L}, B_{1} B_{0}) \leftarrow (AC)$	Outputs the contents of AC to port P(DP <sub>L</sub> ).		
	SPB bit	Set port bit	0 0 0 0	0 1 Bi Bo	1	2	$P(DP_L, B_1 B_0) \leftarrow 1$	Sets to 1 the bit in port $P(DP_L)$ specified by the immediate data $B_1 B_0$ .		Executing this instruction destroys the contents of the E register.
	RPB bit	Reset port bit	0 0 1 0	0 1 B1 B0	1	2	$P(DP_{L}, B_{1} B_{0}) \leftarrow 1$	Clears to 0 the bit in port P(DPL) specified by the immediate data B <sub>1</sub> B <sub>0</sub> .	ZF	Executing this instruction destroys the contents of the E register.
Other instructions	SCTL bit	Set control register bit (S)	0 0 1 0	1 1 0 0	2	2	$CTL \leftarrow (CTL) \lor \\ B_3 B_2 B_1 B_0$	Sets the bit (or bits) in the control register specified by B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> .		
	RCTL bit	Reset control register bit (S)	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	1 1 0 0 B3 B2 B1 B0	2	2	$\begin{array}{c} \text{CTL} \leftarrow (\text{CTL}) \lor \\ B_3 B_2 B_1 B_0 \end{array}$	Clears the bit (or bits) in the control register specified by B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> .	ZF	
	WTTM	Write timer	1 1 1 1	1 0 1 1	1	1	$TM \leftarrow (E), (AC)$ $TMF \leftarrow 0$	Loads the contents of E and AC into the timer. Also clears TMF.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	Stops all operations.		This instruction is disabled only when all bits in port PA are 0.
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	Consumes one machine cycle while performing no operation.		

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