

# LM2755 Charge Pump LED Controller with I<sup>2</sup>C Compatible Interface in DSBGA Package

Check for Samples: [LM2755](#)

## FEATURES

- 90% Peak Efficiency
- Total solution size < 13mm<sup>2</sup>
- No Inductor Required: Only 4 Inexpensive Ceramic Caps
- 3 Independently Controlled Constant Current Outputs
- Programmable Trapezoidal Dimming Waveform on Each Output
- Programmable Timing Control Via Internal Registers and External Clock Synchronization Input
- 32 Exponential Dimming Steps with 800:1 Dimming Ratio

- Programmable Brightness Control via I<sup>2</sup>C-Compatible Interface
- Hardware Enable Pin
- Wide Input Voltage Range: 2.7V to 5.5V
- Tiny 18-bump Thin DSBGA : 1.8mm x 1.6mm x 0.6mm

## APPLICATIONS

- Indicator LEDs
- Keypad LED Backlight
- Display LED Backlight
- Fun-light LEDs

## DESCRIPTION

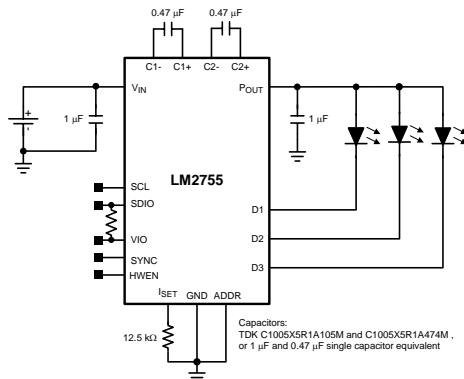
The LM2755 is a charge-pump-based, constant current LED driver capable of driving 3 LEDs with a total output current up to 90mA. The diode current waveforms of each LED can be trapezoidal with timing and level parameters (rise time, fall time, high level, low level, delay, high time, low time) programmed via an I<sup>2</sup>C-compatible interface. The 32 brightness levels found on the LM2755 are exponentially spaced (as opposed to linearly spaced) to better match the response of the human eye to changing brightness levels.

The device requires only four small and low-cost ceramic capacitors. The LM2755 provides excellent efficiency without the use of an inductor by operating the charge pump in a gain of 3/2 or in a gain of 1. Maximum efficiency is achieved over the input voltage range by actively selecting the proper gain based on the LED forward voltage requirements.

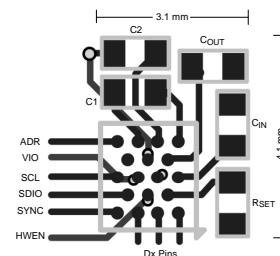
The pre-regulation scheme used by the LM2755 is optimized to ensure low conducted noise on the input. An internal soft-start circuitry eliminates high inrush current at start-up. The LM2755 consumes 3μA (typ.) of supply current in shut-down.

The LM2755 is available in Texas Instruments' tiny 18-bump thin DSBGA package.

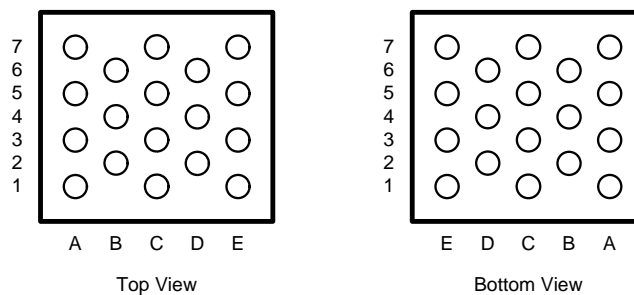
## Typical Application Circuit



**Figure 1. Typical Application Circuit**



## Connection Diagram



**Figure 3. 18-Bump Thin DSBGA Package**  
**1.615mm × 1.807mm × 0.6mm**  
**(See Package Number YFQ0018AAA)**

### PIN DESCRIPTIONS

Pin #s	Pin Names	Pin Descriptions
A1	ID1	LED Driver 1
A3	ID2	LED Driver 2
A5	ID3	LED Driver 3
A7	SYNC	External clock synchronization input
B2	ISSET	LED Driver Current Set Pin
B4	HWEN	Hardware EN Pin. Low '0' = RESET, High '1' = Normal Operation
B6	SDIO	Serial data Input/Output pin
C1	V <sub>IN</sub>	Input Voltage Connection
C3	GND	Ground Connection.
C5	VIO	Serial Bus Voltage Level Input
C7	SCL	Serial Clock Pin
D2	P <sub>OUT</sub>	Charge Pump Output
D4	C2-	Flying Capacitor Connect
D6	GND	Ground connection
E1	C1+	Flying Capacitor Connect
E3	C2+	Flying Capacitor Connect
E5	C1-	Flying Capacitor Connect
E7	ADDR	Chip Address Select Input. VIN = 0x67. Ground = 0x18.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings <sup>(1)(2)(3)</sup>

V <sub>IN</sub> pin voltage	–0.3V to 6.0V
SCL, SDIO, VIO, ADDR, SYNC pin voltages	–0.3V to (V <sub>IN</sub> +0.3V) w/ 6.0V max
I <sub>DX</sub> Pin Voltages	–0.3V to (V <sub>POUT</sub> +0.3V) w/ 6.0V max
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T <sub>J-MAX</sub> )	150°C
Storage Temperature Range	–65°C to +150°C
Maximum Lead Temperature (Soldering)	(5)
ESD Rating <sup>(6)</sup> Human Body Model	2.5kV

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T<sub>J</sub> = 160°C (typ.) and disengages at T<sub>J</sub> = 155°C (typ.).
- (5) For detailed soldering specifications and information, please refer to STET Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112).
- (6) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7)

## Operating Rating <sup>(1)(2)</sup>

Input Voltage Range	2.7V to 5.5V
Junction Temperature (T <sub>J</sub> ) Range	–30°C to 105°C
Ambient Temperature (T <sub>A</sub> ) Range <sup>(3)</sup>	–30°C to +85°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T<sub>A-MAX</sub>) is dependent on the maximum operating junction temperature (T<sub>J-MAX-OP</sub> = 105°C), the maximum power dissipation of the device in the application (P<sub>D-MAX</sub>), and the junction-to ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A-MAX</sub> = T<sub>J-MAX-OP</sub> – (θ<sub>JA</sub> × P<sub>D-MAX</sub>).

## Thermal Properties

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ), YFQ0018 Package <sup>(1)</sup>	56°C/W
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- (1) Junction-to-ambient thermal resistance is highly dependent on application and board layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. For more information, please refer to Texas Instruments STET Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112).

## Electrical Characteristics <sup>(1)(2)</sup>

Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ , and limits in boldface type apply over the full operating temperature range. Unless otherwise specified:  $V_{IN} = 3.6\text{V}$ ;  $V_{D1} = 0.4\text{V}$ ;  $V_{D2} = 0.4\text{V}$ ;  $V_{D3} = 0.4\text{V}$ ;  $R_{SET} = 12.5\text{k}\Omega$ ; D1, D2, and D3 = Fullscale Current; EN1, EN2, and EN3 Bits = "1"; CLK bit = '0';  $C_1 = C_2 = 0.47\mu\text{F}$ ,  $C_{IN} = C_{OUT} = 1\mu\text{F}$ ; Specifications related to output current(s) and current setting pins ( $I_{DX}$  and  $I_{SET}$ ) apply to D1, D2 and D3. <sup>(3)</sup>

Symbol	Parameter	Condition		Min	Typ	Max	Units
I <sub>DX</sub>	Output Current Regulation	3.0V ≤ V <sub>IN</sub> ≤ 5.5V		18.7	20.7	22.7	mA
I <sub>MATCH</sub>	Output Current Matching	3.0V ≤ V <sub>IN</sub> ≤ 5.5V <sup>(4)</sup>			1		%
I <sub>Q</sub>	Quiescent Supply Current	Gain = 3/2 D <sub>1-3</sub> = OPEN, R <sub>SET</sub> = OPEN			1.0	1.3	mA
I <sub>SD</sub>	Shutdown Supply Current	3.0V ≤ V <sub>IN</sub> ≤ 5.5V EN1 = EN2 = EN3 = 0			5	9.5	μA
V <sub>SET</sub>	I <sub>SET</sub> Pin Voltage	3.0V ≤ V <sub>IN</sub> ≤ 5.5V			1.25		V
I <sub>DX</sub> / I <sub>SET</sub>	Output Current to Current Set Ratio	(5)			200		
V <sub>DXTH</sub>	V <sub>DX</sub> 1x to 3/2x Gain Transition Threshold	V <sub>D1</sub> and/or V <sub>D2</sub> and/or V <sub>D3</sub> Falling			350		mV
V <sub>HR</sub>	Current Source Headroom Voltage Requirement <sup>(6)</sup>	I <sub>DX</sub> = 95% × I <sub>DX</sub> (nom.) (I <sub>DX</sub> (nom) ≈ 20mA) Gain = 3/2			200		mV
f <sub>SW</sub>	Switching Frequency			0.975	1.25	1.525	MHz
t <sub>START</sub>	Start-up Time	P <sub>OUT</sub> = 90% steady state			300		μs
f <sub>PWM</sub>	Internal Diode Current PWM Frequency				20		kHz
f <sub>SYNC</sub>	Maximum External Sync Frequency				1.0		MHz
V <sub>HWEN</sub>	HWEN Voltage Thresholds	2.7V ≤ V <sub>IN</sub> ≤ 5.5V	Reset	0		0.5	V
			Normal Operation	1.23		V <sub>IN</sub>	
I <sup>2</sup> C-Compatible Interface Voltage Specifications (SCL, SDIO, VIO)							
V <sub>IO</sub>	Serial Bus Voltage Level	2.7V ≤ V <sub>IN</sub> ≤ 5.5V <sup>(7)</sup>		1.44		V <sub>IN</sub>	V
V <sub>IL</sub>	Input Logic Low "0"	2.7V ≤ V <sub>IN</sub> ≤ 5.5V, V <sub>IO</sub> = 3.0V		0		0.35 × V <sub>IO</sub>	V
V <sub>IH</sub>	Input Logic High "1"	2.7V ≤ V <sub>IN</sub> ≤ 5.5V, V <sub>IO</sub> = 3.0V		0.65 × V <sub>IO</sub>		V <sub>IO</sub>	V
V <sub>OL</sub>	Output Logic Low "0"	I <sub>LOAD</sub> = 3mA				400	mV
I <sup>2</sup> C-Compatible Interface Timing Specifications (SCL, SDIO, VIO) <sup>(8)</sup>							
t <sub>1</sub>	SCL (Clock Period)			2.5			μs
t <sub>2</sub>	Data In Setup Time to SCL High			100			ns
t <sub>3</sub>	Data Out stable After SCL Low			0			ns
t <sub>4</sub>	SDIO Low Setup Time to SCL Low (Start)			100			ns

(1) All voltages are with respect to the potential at the GND pin.

(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

(3)  $C_{IN}$ ,  $C_{OUT}$ ,  $C_1$ , and  $C_2$  : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics

(4) For the current sinks on a part, the following are determined: the maximum sink current in the group (MAX), the minimum sink current in the group (MIN), and the average sink current of the group (AVG). Two matching numbers are calculated:  $(\text{MAX}-\text{AVG})/\text{AVG}$  and  $(\text{AVG}-\text{MIN})/\text{AVG}$ . The larger number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts

(5) The maximum total output current for the LM2755 should be limited to 90mA. The total output current can be split among any of the three banks ( $I_{D1} = I_{D2} = I_{D3} = 30\text{mA Max.}$ ). Under maximum output current conditions, special attention must be given to input voltage and LED forward voltage to ensure proper current regulation. See [MAXIMUM OUTPUT CURRENT](#), [MAXIMUM LED VOLTAGE](#), [MINIMUM INPUT VOLTAGE](#) of the datasheet for more information.

(6) For each  $I_{DX}$  output pin, headroom voltage is the voltage across the internal current sink connected to that pin. For  $V_{HR} = V_{OUT} - V_{Dxx}$ . If headroom voltage requirement is not met, LED current regulation will be compromised.

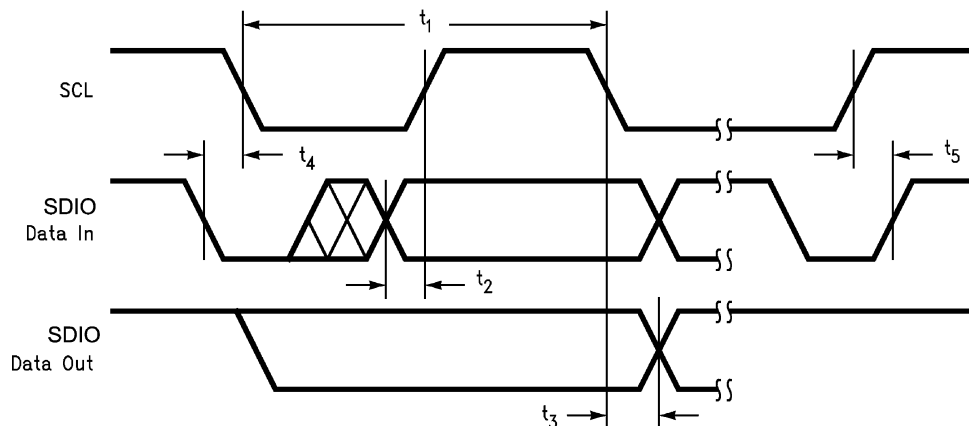
(7) SCL and SDIO signals are referenced to VIO and GND for minimum VIO voltage testing.

(8) SCL and SDIO should be glitch-free in order for proper brightness control to be realized.

## Electrical Characteristics <sup>(1)(2)</sup> (continued)

Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ , and limits in boldface type apply over the full operating temperature range. Unless otherwise specified:  $V_{IN} = 3.6\text{V}$ ;  $V_{D1} = 0.4\text{V}$ ;  $V_{D2} = 0.4\text{V}$ ;  $V_{D3} = 0.4\text{V}$ ;  $R_{SET} = 12.5\text{k}\Omega$ ; D1, D2, and D3 = Fullscale Current; EN1, EN2, and EN3 Bits = "1"; CLK bit = '0';  $C1 = C2 = 0.47\mu\text{F}$ ;  $C_{IN} = C_{OUT} = 1\mu\text{F}$ ; Specifications related to output current(s) and current setting pins ( $I_{DX}$  and  $I_{SET}$ ) apply to D1, D2 and D3. <sup>(3)</sup>

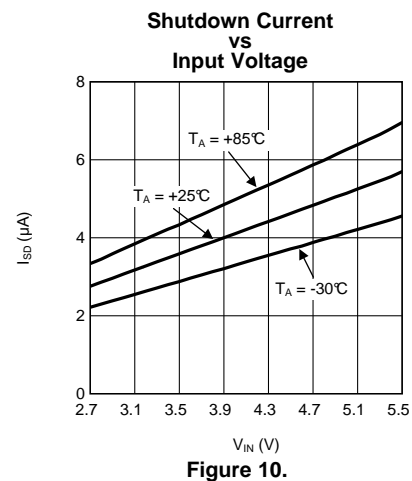
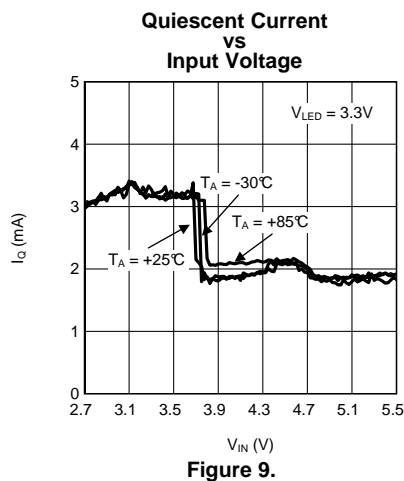
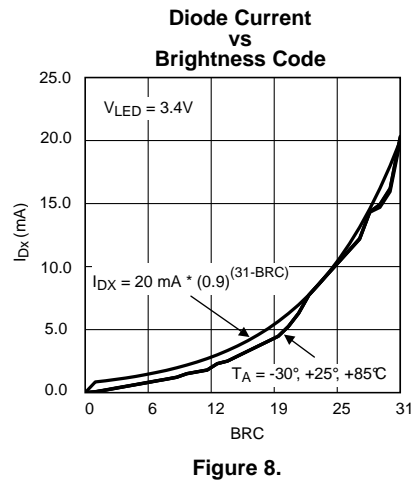
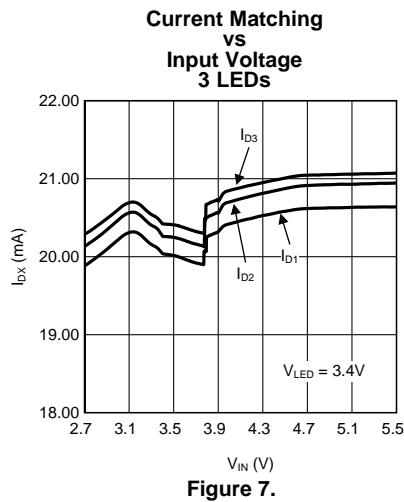
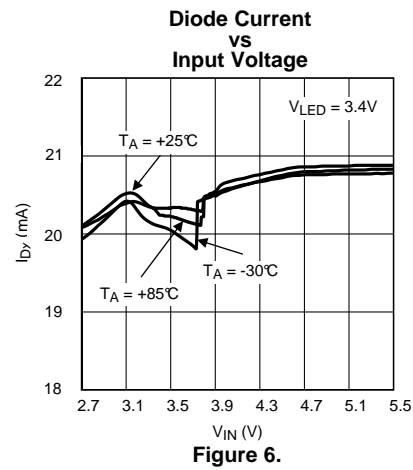
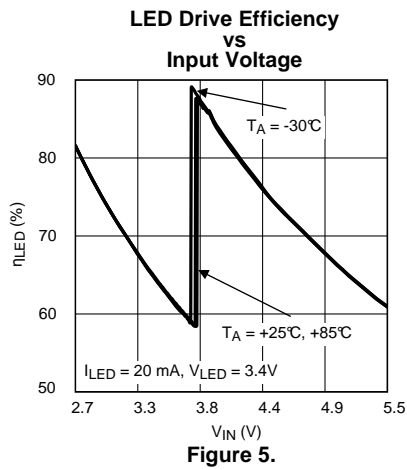
Symbol	Parameter	Condition	Min	Typ	Max	Units
$t_5$	SDIO High Hold Time After SCL High (Stop)		<b>100</b>			ns



**Figure 4. I2C Timing Diagram**

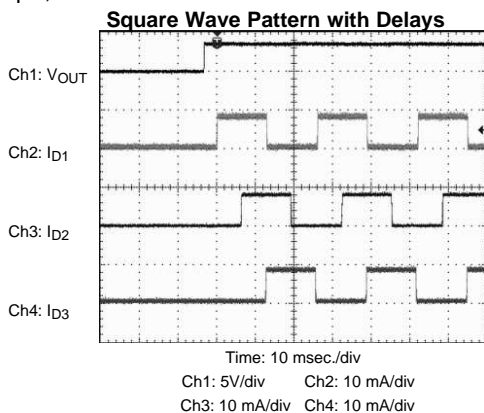
## Typical Performance Characteristics

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ;  $V_{IN} = 3.6\text{V}$ ;  $V_{HWEN} = V_{IN}$ ;  $V_{D1} = V_{D2} = V_{D3} = 3.6\text{V}$ ;  $R_{SET} = 12.5\text{k}\Omega$ ;  $C_1 = C_2 = 0.47\mu\text{F}$ ;  $C_{IN} = C_{VOUT} = 1\mu\text{F}$ ;  $ENA = ENB = ENC = '1'$ .

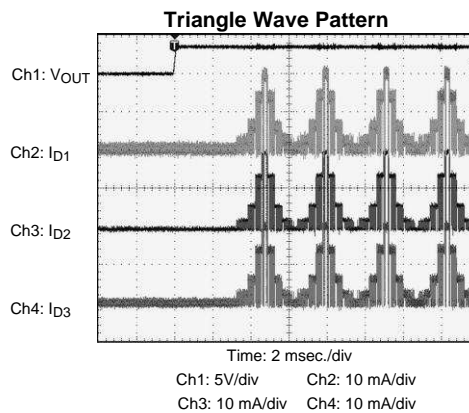


## Typical Performance Characteristics (continued)

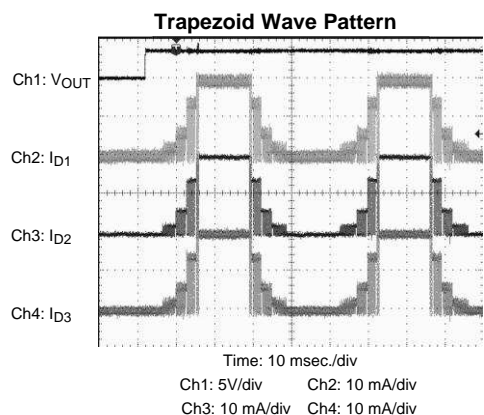
Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ;  $V_{IN} = 3.6\text{V}$ ;  $V_{HVEN} = V_{IN}$ ;  $V_{D1} = V_{D2} = V_{D3} = 3.6\text{V}$ ;  $R_{SET} = 12.5\text{k}\Omega$ ;  $C_1 = C_2 = 0.47\mu\text{F}$ ,  $C_{IN} = C_{VOUT} = 1\mu\text{F}$ ;  $\text{ENA} = \text{ENB} = \text{ENC} = '1'$ .



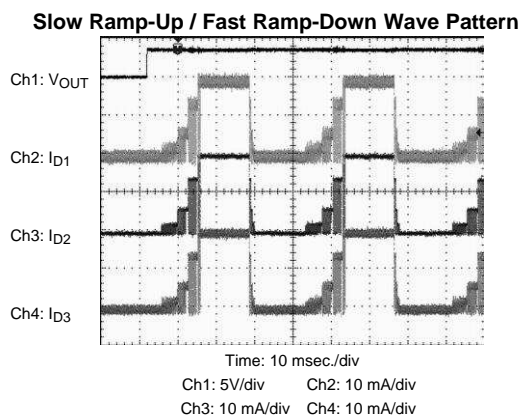
**Figure 11.**



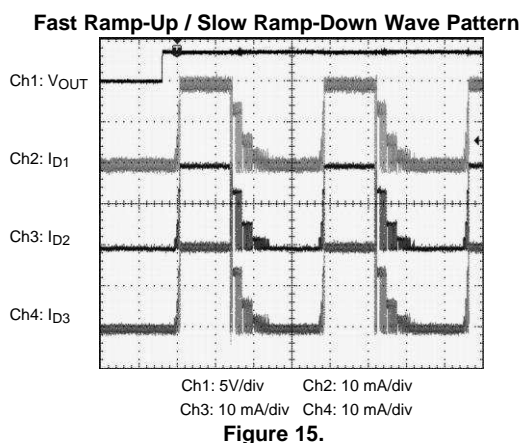
**Figure 12.**



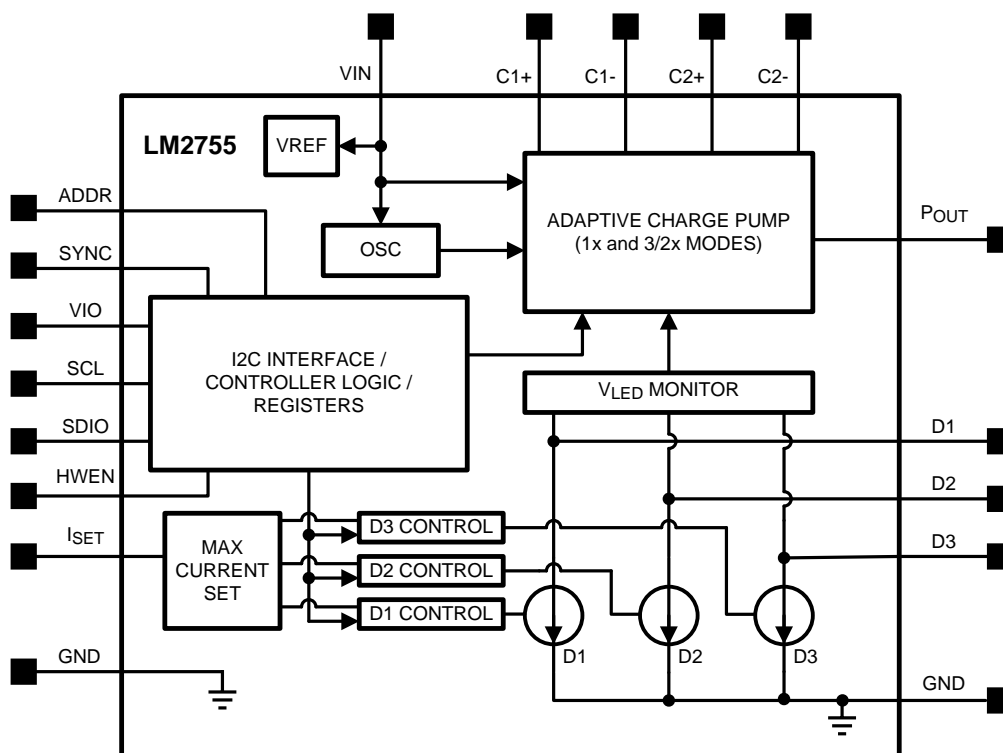
**Figure 13.**



**Figure 14.**



**Figure 15.**

**BLOCK DIAGRAM****Figure 16. Block Diagram**



## CIRCUIT COMPONENTS

### CHARGE PUMP

The input to the 3/2x - 1x charge pump is connected to the  $V_{IN}$  pin, and the regulated output of the charge pump is connected to the  $P_{OUT}$  pin. The recommended input voltage range of the LM2755 is 3.0V to 5.5V. The device's regulated charge pump has both open loop and closed loop modes of operation. When the device is in open loop, the voltage at  $V_{OUT}$  is equal to the gain times the voltage at the input. When the device is in closed loop, the voltage at  $V_{OUT}$  is regulated to 4.6V (typ.). The charge pump gain transitions are actively selected to maintain regulation based on LED forward voltage and load requirements. This allows the charge pump to stay in the most efficient gain (1x) over as much of the input voltage range as possible, reducing the power consumed from the battery.

### LED FORWARD VOLTAGE MONITORING

The LM2755 has the ability to switch converter gains (1x or 3/2x) based on the forward voltage of the LED load. This ability to switch gains maximizes efficiency for a given load. Forward voltage monitoring occurs on all diode pins. At higher input voltages, the LM2755 will operate in pass mode, allowing the  $P_{OUT}$  voltage to track the input voltage. As the input voltage drops, the voltage on the Dx pins will also drop ( $V_{DX} = V_{POUT} - V_{LEDx}$ ). Once any of the active Dx pins reaches a voltage approximately equal to 350mV, the charge pump will then switch to the gain of 3/2x. This switch-over ensures that the current through the LEDs never becomes pinched off due to a lack of headroom on the current sources.

Only active Dx pins will be monitored. For example, if only D1 is enabled, the LEDs connected to D2 and D3 will not affect the gain transition point. If all Dx pins are enabled, all diodes will be monitored, and the gain transition will be based upon the diode with the highest forward voltage.

### HWEN PIN

The LM2755 has a hardware enable/reset pin (HWEN) that allows the device to be disabled by an external controller without requiring an I<sup>2</sup>C write command. Under normal operation, the HWEN pin should be held high (logic '1') to prevent an unwanted reset. When the HWEN is driven low (logic '0'), all internal control registers reset to the default states and the part becomes disabled. Please see [Electrical Characteristics](#) for required voltage thresholds.

### SYNC PIN

The SYNC pin allows the LM2755 to use an external clock to generate the timing within. This allows the LM2755's current-sinks to pulse-width modulate (PWM) and transition at a user controlled frequency. The PWM frequency and the step-time increment can be set by feeding a clock signal into the SYNC pin and enabling bit 6 in the General Purpose register (See [Electrical Characteristics](#) for more details.). The maximum frequency allowed to ensure current level accuracy is 1MHz. This external clock is divided down by 32x to create the minimum time-step and PWM frequency. For a 1MHz external clock, the PWM frequency becomes 31.25KHz, and the minimum step time becomes 32μseconds. If not used, it is recommended that the SYNC pin be tied to ground.

### ADDR PIN

The ADDR pin allows the user to choose between two different I<sup>2</sup>C chip addresses for the LM2755. Tying the ADDR pin high sets the chip address to hex 67 (0x67 or 67h), while tying the ADDR pin low sets the chip address to hex 18 (0x18 or 18h). This feature allows multiple LM2755's to be used within a system in addition to providing flexibility in the event another chip in the system has a chip address similar to the default LM2755 address (0x18).

### I<sup>2</sup>C-Compatible Interface

#### DATA VALIDITY

The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

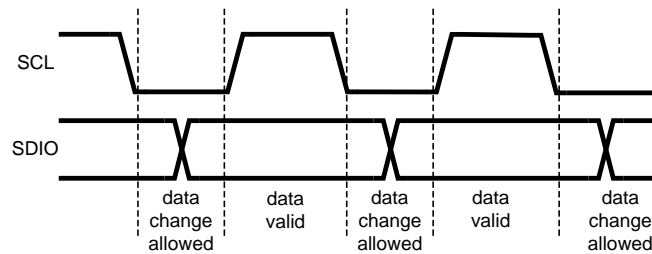


Figure 17. Data Validity Diagram

A pull-up resistor between VIO and SDIO must be greater than  $[(VIO - V_{OL}) / 3mA]$  to meet the  $V_{OL}$  requirement on SDIO. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

### START AND STOP CONDITIONS

START and STOP conditions classify the beginning and the end of the I<sup>2</sup>C session. A START condition is defined as SDIO signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDIO transitioning from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates START and STOP conditions. The I<sup>2</sup>C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I<sup>2</sup>C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

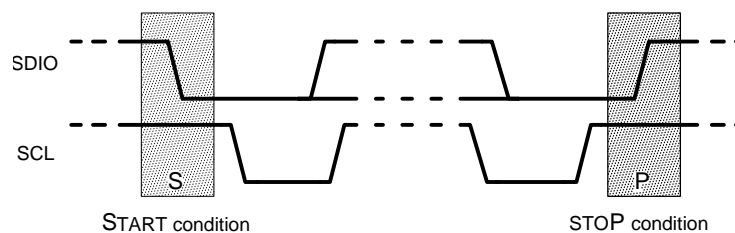


Figure 18. Start and Stop Conditions

### TRANSFERRING DATA

Every byte put on the SDIO line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDIO line (HIGH) during the acknowledge clock pulse. The LM2755 pulls down the SDIO line during the 9th clock pulse, signifying an acknowledge. The LM2755 generates an acknowledge after each byte has been received.

After the START condition, the I<sup>2</sup>C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM2755 address is 18h is ADDR if tied low and 67h if ADDR is tied high. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

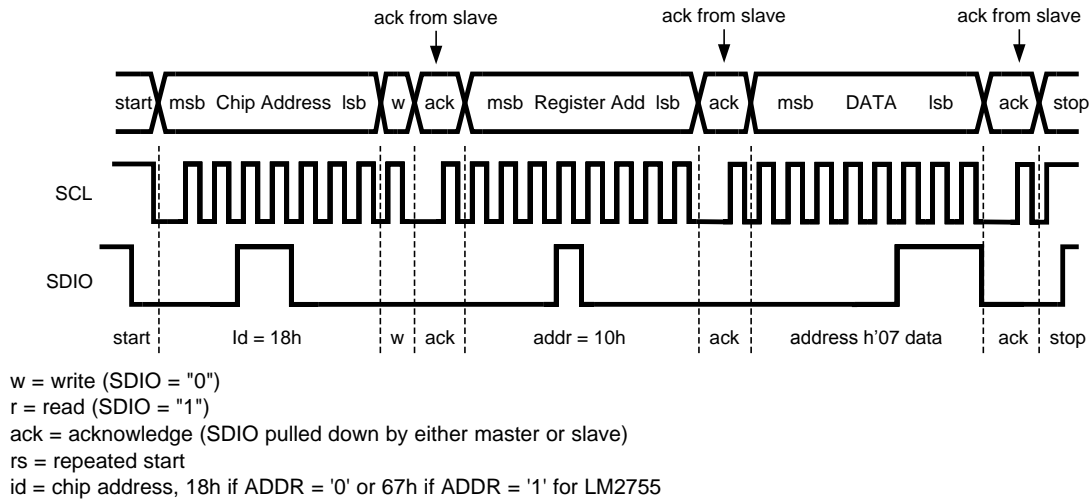


Figure 19. Write Cycle

## I<sup>2</sup>C-COMPATIBLE CHIP ADDRESS

The chip address for LM2755 is 0011000 (0x18) when ADDR = '0' or 1100111 (0x67) when ADDR = '1'.

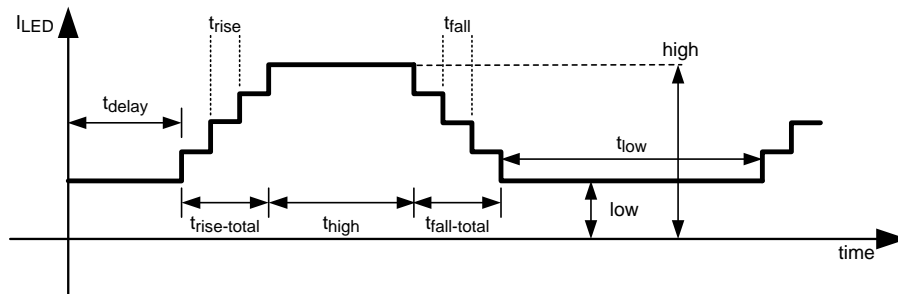


Figure 20. Dimming Waveform

## Internal Registers

Table 1. Internal Registers of LM2755

Register Name	Internal Hex Address	Power On Value
General Purpose	x10	0000 0000
Time Step: n <sub>STEP</sub>	x20	1000 1000
D1 High Level: n <sub>ID1H</sub>	xA9	1110 0000
D1 Low Level: n <sub>ID1L</sub>	xA8	1110 0000
D1 Delay: n <sub>delay1</sub>	xA1	0000 0000
D1 Ramp-Up Step Time: n <sub>rise1</sub>	xA5	0000 0000 <sup>(1)</sup>
D1 Time High: n <sub>high1</sub>	xA3	0000 0000
D1 Ramp-Down Step Time: n <sub>fall1</sub>	xA4	0000 0000 <sup>(1)</sup>
D1 Timing: n <sub>low1</sub>	xA2	0000 0000
D2 High Level: n <sub>ID2H</sub>	xB9	1110 0000
D2 Low Level: n <sub>ID2L</sub>	xB8	1110 0000
D2 Delay: n <sub>delay2</sub>	xB1	0000 0000
D2 Ramp-Up Step Time: n <sub>rise2</sub>	xB5	0000 0000 <sup>(1)</sup>

(1) n<sub>rise</sub> or n<sub>fall</sub> = 0 or 1 are not valid and should not be used

**Table 1. Internal Registers of LM2755 (continued)**

Register Name	Internal Hex Address	Power On Value
D2 Time High: $n_{\text{high}2}$	xB3	0000 0000
D2 Ramp-Down Step Time: $n_{\text{fall}2}$	xB4	0000 0000 <sup>(1)</sup>
D2 Timing: $n_{\text{low}2}$	xB2	0000 0000
D3 High Level: $n_{\text{ID}3\text{H}}$	xC9	1110 0000
D3 Low Level: $n_{\text{ID}3\text{L}}$	xC8	1110 0000
D3 Delay: $n_{\text{delay}3}$	xC1	0000 0000
D3 Ramp-Up Step Time: $n_{\text{rise}3}$	xC5	0000 0000 <sup>(1)</sup>
D3 Time High: $n_{\text{high}3}$	xC3	0000 0000
D3 Ramp-Down Step Time: $n_{\text{fall}3}$	xC4	0000 0000 <sup>(1)</sup>
D3 Timing: $n_{\text{low}3}$	xC2	0000 0000

**GENERAL PURPOSE REGISTER DESCRIPTION**

- Bit 0: enable output D1 with high current level.
- Bit 1: enable output D2 with high current level.
- Bit 2: enable output D3 with high current level.
- Bit 3: enable dimming waveform on output D1.
- Bit 4: enable dimming waveform on output D2.
- Bit 5: enable dimming waveform on output D3.
- Bit 6: enable external clock. '1' = External Clock Sync, '0' = Internal Clock Used
- Bit 7: If Bit 7 = 0 the charge pump is powered on before any dimming waveform is enabled. It is recommended that Bit7 be set to a '0' if an external clock is used. If Bit 7 = 1 the dimming waveform can be enabled before charge pump is powered on.

**Application Information****SETTING FULL-SCALE LED CURRENT**

The current through the LEDs connected to D1, D2 and D3 can be set to a desired level simply by connecting an appropriately sized resistor ( $R_{\text{SET}}$ ) between the ISET pin of the LM2755 and GND. The LED currents are proportional to the current that flows through the ISET pin and are a factor of 200 times greater than the  $I_{\text{SET}}$  currents. The feedback loop of the internal amplifier sets the voltage of the ISET pin to 1.25V (typ.). The statement above is simplified in the equation below:

$$I_{\text{Dx (Full-Scale)}} = 200 \times (V_{\text{ISET}} / R_{\text{SET}}) \quad (1)$$

Please refer to **I<sup>2</sup>C-Compatible Interface** for detailed instructions on how to adjust the brightness control registers.

**BRIGHTNESS LEVEL CONTROL**

Once the desired  $R_{\text{SET}}$  value has been chosen, the LM2755 can internally dim the LEDs by modulating the currents with an internally set 20kHz PWM signal. The PWM duty cycle percentage is independently set for each LED through the I<sup>2</sup>C-compatible interface. The 32 brightness levels follow a exponentially increasing pattern rather than a linearly increasing one in order to better match the human eye's response to changing brightness. The brightness level response is modeled in the following equations.:

$$I_{\text{Dx LOW}} = (0.9)^{(31-n_{\text{IDxL}})} \times I_{\text{Dx Fullscale}} \quad (2)$$

$$I_{\text{Dx HIGH}} = (0.9)^{(31-n_{\text{IDxH}})} \times I_{\text{Dx Fullscale}} \quad (3)$$

$n_{\text{IDxH}}$  and  $n_{\text{IDxL}}$  are numbers between 0 and 31 stored in the Brightness Level registers. When the waveform enable bits are set to '1',  $n_{\text{IDxH}}$  and  $n_{\text{IDxL}}$  are the brightness level boundaries. These equations apply to all Dx outputs and their corresponding registers. A '0' code in the Brightness Control register sets the current to an "off-state" (0mA).

## TIME STEP CONTROL

Bit 0 to Bit 2: The value of these 3 bits is equal to N, which is used in the timing control equations ( $0 \leq N \leq 7$ ). The minimum internal time step ( $N=0$ ) is  $50\mu\text{s}$ . Setting the time-step to  $N=7$  results in a maximum time step of  $6.4\text{msec}$ .

$$t_{\text{STEP}} = 50\mu\text{sec} \times 2^{N_{\text{STEP}}} \text{ if the internal clock is used.} \quad (4)$$

$$t_{\text{STEP}} = 2^{N_{\text{STEP}}} \times (32 \div f_{\text{SYNC}}) \text{ if the external clock on the SYNC pin is used.} \quad (5)$$

Bit 3 to Bit 7: Not used

## DELAY CONTROL

The LM2755 allows the programmed current waveform on each diode pin to independently start with a delay upon enabling the waveform dimming bits in the general purpose register. There are 256 delay levels available. The delay time is set by the following equation:

$$\text{For } n_{\text{STEP}} = 0, t_{\text{delayx}} = t_{\text{STEP}} \times (n_{\text{delayx}} + n_{\text{risex}}) \text{ By default, } n_{\text{delayx}} = 0 \text{ with a range of } 0 \leq n_{\text{delay}} \leq 255. \text{ For } 1 \leq n_{\text{STEP}} \leq 7, t_{\text{delayx}} = t_{\text{STEP}} \times [(n_{\text{delayx}} - 1) + (n_{\text{risex}} - 1)]$$

where

- $1 \leq n_{\text{delay}} \leq 255$ .
- If  $n_{\text{delay}} = 0$ ,  $t_{\text{delayx}} = 0\text{s}$ .
- $n_{\text{delayx}}$  is stored in the Dx Delay registers. (6)

## TIMING CONTROL

$n_{\text{risex}}$ ,  $n_{\text{fallx}}$ ,  $n_{\text{highx}}$ ,  $n_{\text{lowx}}$  are numbers between 0 and 255, stored in the timing control registers. The durations of the rise, high, fall and low times are given by:

$$\text{For } n_{\text{STEP}} = 0, t_{\text{rise/fall}} = t_{\text{STEP}} \times (n_{\text{IDxH}} - n_{\text{IDxL}} - 1) \times n_{\text{risex/fallx}}$$

where

- $2 \leq n_{\text{risex/fallx}} \leq 255$   **$n_{\text{risex}}$  or  $n_{\text{fallx}} = 0$  or 1 are not valid and should not be used** (7)

$$\text{For } 1 \leq n_{\text{STEP}} \leq 7, t_{\text{rise/fall}} = t_{\text{STEP}} \times (n_{\text{IDxH}} - n_{\text{IDxL}} - 1) \times (n_{\text{risex/fallx}} - 1)$$

where

- $2 \leq n_{\text{risex/fallx}} \leq 255$   **$n_{\text{risex}}$  or  $n_{\text{fallx}} = 0$  or 1 are not valid and should not be used** (8)

$$\text{For } n_{\text{STEP}} = 0, t_{\text{highx}} = t_{\text{STEP}} \times (n_{\text{highx}} + n_{\text{fallx}}) \quad t_{\text{lowx}} = t_{\text{STEP}} \times (n_{\text{lowx}} + n_{\text{risex}})$$

where

- $1 \leq n_{\text{highx/lowx}} \leq 255$  For  $n_{\text{highx/lowx}}=0$ ,  $t_{\text{high}}$  or  $t_{\text{low}} = t_{\text{STEP}}$  (9)

$$\text{For } 1 \leq n_{\text{STEP}} \leq 7, t_{\text{highx}} = t_{\text{STEP}} \times ((n_{\text{highx}} - 1) + (n_{\text{fallx}} - 1)) \quad t_{\text{lowx}} = t_{\text{STEP}} \times ((n_{\text{lowx}} - 1) + (n_{\text{risex}} - 1))$$

where

- $2 \leq n_{\text{highx/lowx}} \leq 255$  For  $n_{\text{highx/lowx}} = 0$  or 1,  $t_{\text{highx}} = t_{\text{STEP}} \times (n_{\text{fallx}} - 1) \quad t_{\text{lowx}} = t_{\text{STEP}} \times (n_{\text{risex}} - 1)$  (10)

## SYNC PIN TIMING CONTROL

It is possible to replace the internal clock with an external one placed on the external SYNC pin. Writing a '1' to bit 6 in the General Purpose register switches the system clock from being internally generated to externally generated. The frequency of the PWM modulating signal becomes:

$$f_{\text{PWM}} = f_{\text{SYNC}} / 32 \quad (11)$$

The maximum recommended SYNC frequency is 1MHz. This frequency yields a PWM frequency of 31.25KHz and the minimum step time of  $32\mu\text{sec}$ .

## MAXIMUM OUTPUT CURRENT, MAXIMUM LED VOLTAGE, MINIMUM INPUT VOLTAGE

The LM2755 can drive 3 LEDs at 30mA each (D1, D2, D3) from an input voltage as low as 3.2V, as long as the LEDs have a forward voltage of 3.6V or less (room temperature).

The statement above is a simple example of the LED drive capability of the LM2755. The statement contains the key application parameters that are required to validate an LED-drive design using the LM2755: LED current ( $I_{\text{LEDx}}$ ), number of active LEDs ( $N_x$ ), LED forward voltage ( $V_{\text{LED}}$ ), and minimum input voltage ( $V_{\text{IN-MIN}}$ ).

The equation below can be used to estimate the maximum output current capability of the LM2755:

$$I_{LED\_MAX} = [(1.5 \times V_{IN}) - V_{LED} - (I_{ADDITIONAL} \times R_{OUT})] \div [(N_x \times R_{OUT}) + k_{HRx}] \quad (12)$$

$$I_{LED\_MAX} = [(1.5 \times V_{IN}) - V_{LED} - (I_{ADDITIONAL} \times 2.4\Omega)] \div [(N_x \times 2.4\Omega) + k_{HRx}]$$

- $I_{ADDITIONAL}$  is the additional current that could be delivered to the other LED Groups. (13)

**R<sub>OUT</sub>**: Output resistance. This parameter models the internal losses of the charge pump that result in voltage droop at the pump output  $V_{OUT}$ . Since the magnitude of the voltage droop is proportional to the total output current of the charge pump, the loss parameter is modeled as a resistance. The output resistance of the LM2755 is typically 2.4Ω ( $V_{IN} = 3.6V$ ,  $T_A = 25^\circ C$ ). In equation form:

$$V_{OUT} = (1.5 \times V_{IN}) - [(I_{LED1} + I_{LED2} + I_{LED3}) \times R_{OUT}] \quad (14)$$

**k<sub>HR</sub>** – Headroom constant. This parameter models the minimum voltage required to be present across the current sinks for them to regulate properly. This minimum voltage is proportional to the programmed LED current, so the constant has units of mV/mA. The typical  $k_{HR}$  of the LM2755 is 3.25mV/mA. In equation form:

$$(V_{OUT} - V_{LEDx}) > k_{HRx} \times I_{LEDx} \quad (15)$$

$$\text{Typical Headroom Constant Values } k_{HR1} = k_{HR2} = k_{HR3} = 10 \text{ mV/mA} \quad (16)$$

The " $I_{LED\_MAX}$ " Equation 12 is obtained from combining the " $R_{OUT}$ " Equation 14 with the " $k_{HRx}$ " Equation 15 and solving for  $I_{LEDx}$ . Maximum LED current is highly dependent on minimum input voltage and LED forward voltage. Output current capability can be increased by raising the minimum input voltage of the application, or by selecting an LED with a lower forward voltage. Excessive power dissipation may also limit output current capability of an application.

### Total Output Current Capability

The maximum output current that can be drawn from the LM2755 is 90mA. Each driver group has a maximum allotted current per Dx sink that must not be exceeded.

**Table 2.**

DRIVER TYPE	MAXIMUM Dx CURRENT
Dx	30mA per Dx Pin

The 90mA load can be distributed in many different configurations. Special care must be taken when running the LM2755 at the maximum output current to ensure proper functionality.

### POWER EFFICIENCY

Efficiency of LED drivers is commonly taken to be the ratio of power consumed by the LEDs ( $P_{LED}$ ) to the power drawn at the input of the part ( $P_{IN}$ ). With a 3/2x - 1x charge pump, the input current is equal to the charge pump gain times the output current (total LED current). The efficiency of the LM2755 can be predicted as follow:

$$P_{LEDTOTAL} = (V_{LEDA} \times N_A \times I_{LEDA}) + (V_{LEDB} \times N_B \times I_{LEDB}) + (V_{LEDC} \times I_{LEDC}) \quad (17)$$

$$P_{IN} = V_{IN} \times I_{IN} \quad (18)$$

$$P_{IN} = V_{IN} \times (GAIN \times I_{LEDTOTAL} + I_Q) \quad (19)$$

$$E = (P_{LEDTOTAL} \div P_{IN}) \quad (20)$$

The LED voltage is the main contributor to the charge-pump gain selection process. Use of low forward-voltage LEDs (3.0V to 3.5V) will allow the LM2755 to stay in the gain of 1x for a higher percentage of the lithium-ion battery voltage range when compared to the use of higher forward voltage LEDs (3.5V to 4.0V). See [LED FORWARD VOLTAGE MONITORING](#) for a more detailed description of the gain selection and transition process.

For an advanced analysis, it is recommended that power consumed by the circuit ( $V_{IN} \times I_{IN}$ ) for a given load be evaluated rather than power efficiency.

### POWER DISSIPATION

The power dissipation ( $P_{DISS}$ ) and junction temperature ( $T_J$ ) can be approximated with the equations below.  $P_{IN}$  is the power generated by the 3/2x - 1x charge pump,  $P_{LED}$  is the power consumed by the LEDs,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance for the DSBGA 18-bump package.  $V_{IN}$  is the input voltage to the LM2755,  $V_{LED}$  is the nominal LED forward voltage,  $N$  is the number of LEDs and  $I_{LED}$  is the programmed LED current.

$$P_{DISS} = P_{IN} - P_{LED1} - P_{LED2} - P_{LED3} \quad (21)$$

$$P_{DISS} = (GAIN \times V_{IN} \times I_{D1 + D2 + D3}) - (V_{LED1} \times I_{LED1}) - (V_{LED2} \times I_{LED2}) - (V_{LED3} \times I_{LED3}) \quad (22)$$

$$T_J = T_A + (P_{DISS} \times \theta_{JA}) \quad (23)$$

The junction temperature rating takes precedence over the ambient temperature rating. The LM2755 may be operated outside the ambient temperature rating, as long as the junction temperature of the device does not exceed the maximum operating rating of 105°C. The maximum ambient temperature rating must be derated in applications where high power dissipation and/or poor thermal resistance causes the junction temperature to exceed 105°C.

## THERMAL PROTECTION

Internal thermal protection circuitry disables the LM2755 when the junction temperature exceeds 160°C (typ.). This feature protects the device from being damaged by high die temperatures that might otherwise result from excessive power dissipation. The device will recover and operate normally when the junction temperature falls below 155°C (typ.). It is important that the board layout provide good thermal conduction to keep the junction temperature within the specified operating ratings.

## CAPACITOR SELECTION

The LM2755 requires 4 external capacitors for proper operation ( $C_{IN} = C_{OUT} = 1\mu F$ ,  $C_1 = C_2 = 0.47\mu F$ ). Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR <20mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM2755 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM2755. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over -55°C to 125°C; X5R: ±15% over -55°C to 85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2755. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, -20%) and vary significantly over temperature (Y5V: +22%, -82% over -30°C to +85°C range; Z5U: +22%, -56% over +10°C to +85°C range). Under some conditions, a nominal 1μF Y5V or Z5U capacitor could have a capacitance of only 0.1μF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2755.

**The recommended voltage rating for the capacitors is 10V to account for DC bias capacitance losses.**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2755TM/NOPB	ACTIVE	DSBGA	YFQ	18	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D32	<a href="#">Samples</a>
LM2755TMX/NOPB	ACTIVE	DSBGA	YFQ	18	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D32	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2755TM/NOPB	DSBGA	YFQ	18	250	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LM2755TMX/NOPB	DSBGA	YFQ	18	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2755TM/NOPB	DSBGA	YFQ	18	250	203.0	190.0	41.0
LM2755TMX/NOPB	DSBGA	YFQ	18	3000	206.0	191.0	90.0



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