LM4970 Boomer® Audio Power Amplifier Series Audio Synchronized Color LED Driver

Check for Samples: LM4970

FEATURES

- **Audio Synchronized Color LED Driver**
- **User Defined LED Pattern, Color, and Intensity Capability**
- **Programmable:**
  - **LED Drive Current**
  - **PWM Frequency**
  - **High Pass Filter Frequency Select**
  - **Audio Input Signal Gain**
- **Eliminates External LED Current Limiting Resistors**
- **I^2C Compatible Interface**
- **Ultra Low Shutdown Current**

APPLICATIONS

- **Cell Phones**
- **Portable MP3, CD, DVD, AAC players**
- **PDA's**

KEY SPECIFICATIONS

- **LED Drive Current per Channel (V_{DD} = 5V): 42mA (2X Setting)**
- **Shutdown Current, V_{DD} = 5V: 1.5µA (Typ)**

DESCRIPTION

The LM4970 is a LED driver with an audio synchronization mode that virtually eliminates the need for real time software processing for LED lighting effects. The LM4970 includes three individual PWM color LED drivers that provide up to 42mA of current drive for each PWM LED output.

The LM4970 features an audio synchronization mode where the audio input signal that is mixed in from three audio inputs is filtered into three frequency bands, with each frequency band assigned to a specific PWM LED driver.

The PWM LED drivers can also be directly programmed through an I^2C compatible interface for applications where user defined LED pattern, color, and intensity programmability is a priority.

The LM4970 also features an audio input gain control which allows the user to increase the gain if the audio input signal does not create a bright enough effect on the LEDs. The LM4970 is a feature rich LED driver that is available in a space saving 14 pin non-pullback WSON package.

Block Diagram

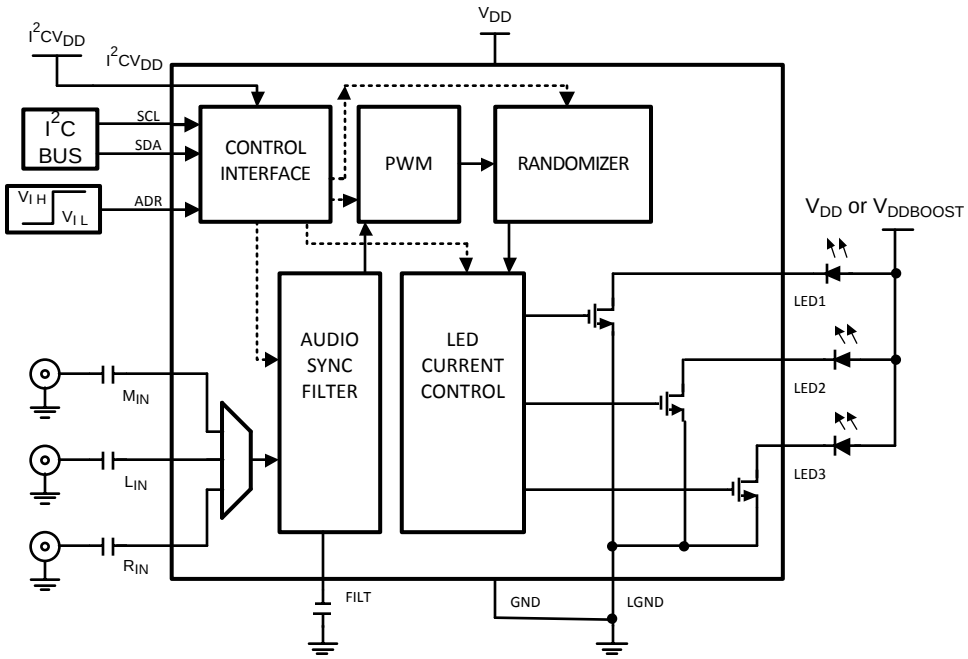


Figure 1. Block Diagram

Connection Diagram

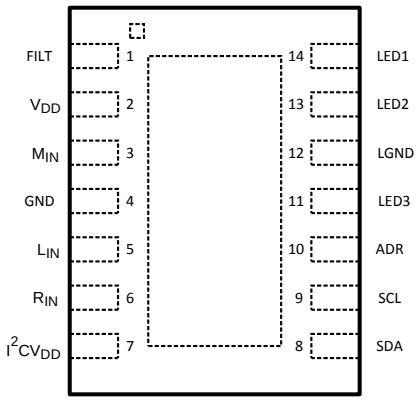


Figure 2. 14 pin NHK Package (Top View)
See Package Number NHK0014A

PIN DESCRIPTIONS

Pin	Name	Pin Description
1	FILT	Low Pass Filter Input
2	V_{DD}	Power Supply Pin
3	M_{IN}	Mono Audio Input
4	GND	Ground
5	L_{IN}	Left Audio Input
6	R_{IN}	Right Audio Input
7	I^2CV_{DD}	I^2C Interface Power Supply
8	SDA	I^2C Data
9	SCL	I^2C Clock
10	ADR	I^2C Address Select
11	LED3	LED output 3
12	LGND	LED ground
13	LED2	LED output 2
14	LED1	LED output 1

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation(4)		Internally Limited
ESD Susceptibility(5)		2000V
ESD Susceptibility(6)		200V
ESD Susceptibility(7)		100V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (NHK0014A)(8)	57°C/W
	θ_{JC} (NHK0014A)	12°C/W

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which specify specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) Machine Model, 200pF–220pF discharged through all pins, except pins 13 and 14.
(7) Machine Model, 200pF–220pF discharge through pins 13 and 14 (LED1 and LED2).
(8) The given θ_{JA} is for an LM4970SD mounted on a PCB with a $2in^2$ area of 1oz printed circuit board copper ground plane.

Operating Ratings

Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)	$-40°C \le T_A \le +85°C$
Supply Voltage	$2.7V \le V_{DD} \le 5.5V$(1)
	$2.5V \le I^2CV_{DD} \le 5.5V$

(1) V_{DD} may be used to power the LEDs. It may be necessary to drive the LEDs from a boost ($V_{DDBOOST}$) found within the system.

Control Interface Electrical Characteristics[1][2]

The following specifications apply for 3V ≤ V_{DD} ≤ 5V unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4970		Units (Limits)
			Typical[3]	Limits[4][5]	
t_1	SCL period			2.5	µs (min)
t_2	SDA Setup Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
V_{IH}	Digital Input High Voltage			0.7 x I^2CV_{DD}	V (min)
V_{IL}	Digital Input Low Voltage			0.3 x I^2CV_{DD}	V (max)

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which specify specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at +25°C and represent the parametric norm.
(4) Limits are ensured to AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

Color LED Driver Electrical Characteristics V_{DD} = 5.0V[1][2][3]

The following specifications apply for V_{DD} = 5.0V unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4970		Units (Limits)
			Typical[4]	Limits[5][6]	
I_{DDRGB}	Supply Curent		2.5	4	mA (max)
I_{SDRGB}	Shutdown Current	Shutdown Mode	1.5	3.5	µA (max)
I_{LED}	LED Drive Current	.66X current drive setting	14		mA
		1X current drive setting	21		mA
		1.33X current drive setting	30		mA
		2X current drive setting	42	23	mA (min)
f_{PWM}	PWM Frequency	PWM_F<1:0> = '01'	60		Hz
	Input Signal Level Gain Control	Maximum setting	12		dB
		Minimum setting	–11		dB

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which specify specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Shutdown current and supply current are measured in a normal room environment. All digital input pins are connected to I^2CV_{DD}.
(4) Typicals are measured at +25°C and represent the parametric norm.
(5) Limits are ensured to AOQL (Average Outgoing Quality Level).
(6) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

Color LED Driver Electrical Characteristics V_{DD} = 3.0V (1)(2)(3)

The following specifications apply for V_{DD} = 3.0V unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4970		Units (Limits)
			Typical (4)	Limits (5)(6)	
I_{DDRGB}	Supply Curent		2.2	3	mA (max)
I_{SDRGB}	Shutdown Current (3)	Shutdown Mode	0.5	2	µA (max)
I_{LED}	LED Drive Current	.66X current drive setting	12		mA
		1X current drive setting	18		mA
		1.33X current drive setting	27		mA
		2X current drive setting	35	21	mA (min)
f_{PWM}	PWM Frequency	PWM_F<1:0> = '01'	60		Hz
	Input Signal Level Gain Control	Maximum setting	12		dB
		Minimum setting	–11		dB

(1) All voltages are measured with respect to the GND pin unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which specify specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Shutdown current and supply current are measured in a normal room environment. All digital input pins are connected to I^2CV_{DD}.
(4) Typicals are measured at +25°C and represent the parametric norm.
(5) Limits are ensured to AOQL (Average Outgoing Quality Level).
(6) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

External Components Description

Components		Functional Description
1.	C_i	This is the input coupling capacitor. It blocks the DC voltage and couples the input signal to the amplifier's input terminals. C_{IN} also creates a highpass filter with an internal 20kΩ resistor at $f_c = 1/(2\pi.20000.C_i)$.
2.	C_S	This is the supply bypass capacitor. It filters the supply voltage applied to the V_{DD} pin and helps reduce the noise at the V_{DD} pin.
3.	C_{filt}	This capacitor creates a low pass filter with an internal 4kΩ resistor at $f_c = 1/(2\pi*4000*C_{filt})$. This pole set at f_c determines the high cutoff frequency for the low band PWM color LED driver output, LED1.

Typical Performance Characteristics(1)

Audio Sync LED Frequency Response (Left - lowband, Mid - midband, Right - highband) (Cfilt = 0.047µF, HPF = 3.5kHz setting)

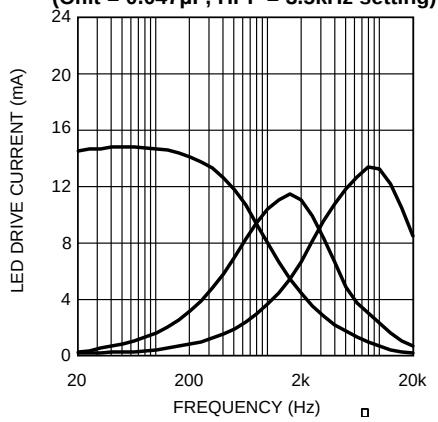


Figure 3.

Audio Sync LED Frequency Response (Left - lowband, Mid - midband, Right - highband) (Cfilt = 0.068µF, HPF = 3.5kHz setting)

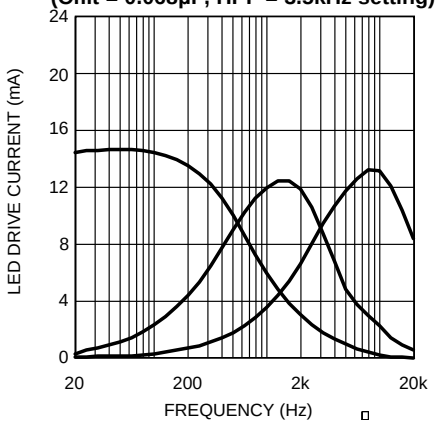


Figure 4.

Audio Sync LED Frequency Response (Left - lowband, Mid - midband, Right - highband) (Cfilt = 0.1µF, HPF = 3.5kHz setting)

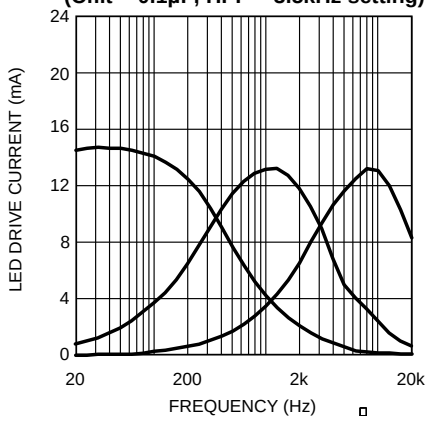


Figure 5.

Audio Sync LED Frequency Response (Left - lowband, Mid - midband, Right - highband) (Cfilt = 0.22µF, HPF = 3.5kHz setting)

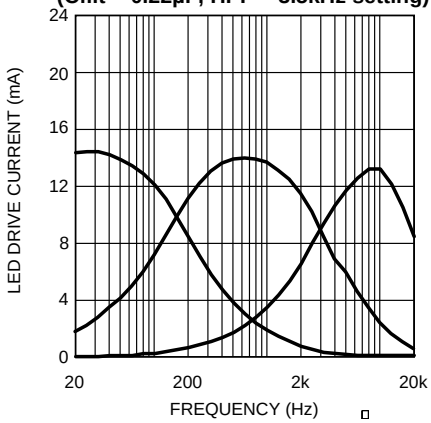


Figure 6.

Audio Sync LED Frequency Response (Left - lowband, Mid - midband, Right - highband) (Cfilt = 0.47µF, HPF = 3.5kHz setting)

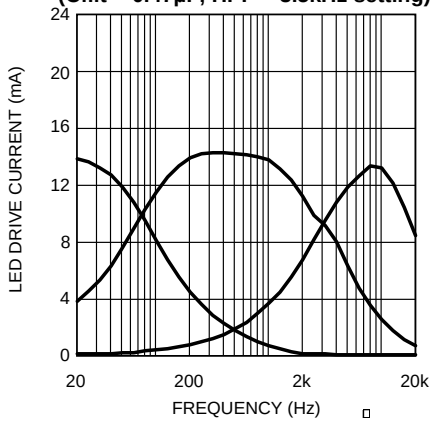


Figure 7.

Audio Sync LED Frequency Response (Left - lowband, Mid - midband, Right - highband) (Cfilt = 0.68µF, HPF = 3.5kHz setting)

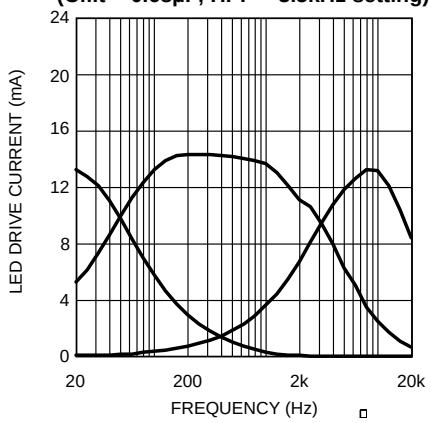


Figure 8.

(1) Audio input level set at $1V_{RMS}$. The input summing amplifier gain is set to 12dB.

Typical Performance Characteristics[1] (continued)

Audio Sync LED Frequency Response (Left - lowband, Mid - midband, Right - highband) (Cfilt = 1µF, HPF = 3.5kHz setting)

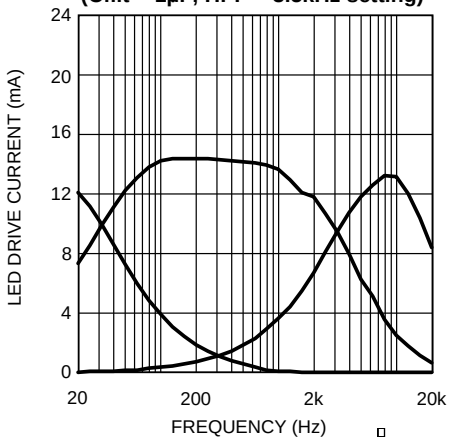


Figure 9.

Audio Sync LED Frequency Response (Left - lowband, Mid - midband, Right - highband) (Cfilt = 2.2µF, HPF = 3.5kHz setting)

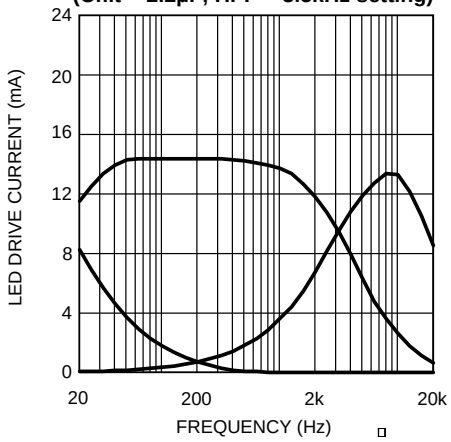


Figure 10.

Highpass Filter Frequency Response vs HPF_F<1:0> setting (Top - 3.5kHz setting, Mid - 6.3kHz setting, Bot -8.9kHz setting)

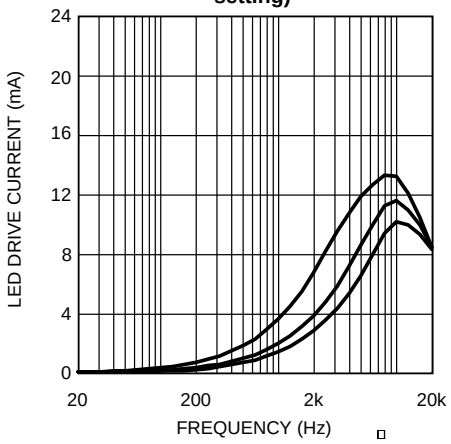


Figure 11.

Low Pass Filter Frequency Responsevs Cfilt (From Left to Right: Cfilt (µF) = 2.2, 1.0, 0.68, 0.47, 0.22, 0.1, 0.068, 0.047, No Cfilt)

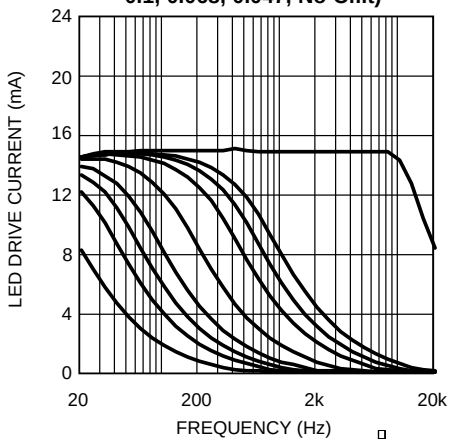


Figure 12.

APPLICATION INFORMATION

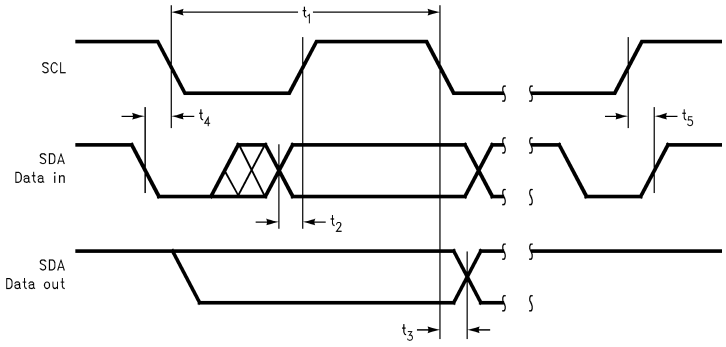


Figure 13. I²C Timing Diagram

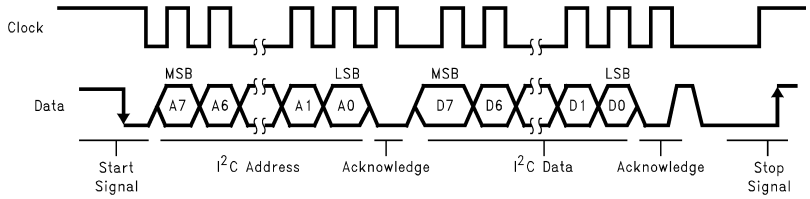


Figure 14. I²C Bus Format

Table 1. Color LED Driver Chip Address (1)

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	0	1	EC	0
ADR = 0	1	1	1	1	0	1	0	0
ADR = 1	1	1	1	1	0	1	1	0

(1) EC - externally configured by ADR pin

Table 2. Color LED Driver Control Registers

Register Name	D7	D6	D5	D4	D3	D2	D1	D0
Mode Select	0	0	0	MS4	MS3	MS2	MS1	MS0
Frequency Select	0	1	0	FS4	FS3	FS2	FS1	FS0
Pattern Select	0	1	1	PS4	PS3	PS2	PS1	PS0
Current Select	1	0	CS5	CS4	CS3	CS2	CS1	CS0
Gain Select	1	1	GS5	GS4	GS3	GS2	GS1	GS0

Table 3. Mode Select Register

Data Bit	Bit Name	Default Value	Condition	Function
MSO	I²C_SD	1	0	Enables device power up mode
			1	Enables device shutdown mode
MS1	I²C_RST	0	0	Enables device normal operation
			1	Enables device RESET, excluding the I²C register settings
MS2	RAND	1	0	Disables the audio synchronization randomizer
			1	Enables the audio synchronization randomizer
MS3	RSVD	0	0	RESERVED
			1	
MS4	RSVD	0	0	RESERVED
			1	

Table 4. Frequency Select Register

Data Bit	Bit Name	Default Value	Condition	Function	
FSO	PWM_FO	0	0	Programs the oscillation frequency of the PWM. PWM oscillation frequency is set as follows:	
			1	**PWM_F<1:0>**	**PWM Frequency**
FS1	PWM_F1	0	0	00	15kHz
				01	60Hz
			1	10	7Hz
				11	4Hz
FS2	RSVD	0	0	RESERVED	
			1		
FS3	HPF_FO	0	0	Programs the internal high pass filter cutoff frequency. High pass filter cutoff frequency is set as follows:	
			1		
FS4	HPF_F1	1	0	HPF_F<1:0>	High Pass Filter Cutoff Frequency
			1	00	3.5kHz
				01	6.3kHz
				10	6.3kHz
				11	8.9kHz

Table 5. Pattern Select Register

Data Bit	Bit Name	Default Value	Condition	Function
PSO	I^2C_SEL	0	0	Enables LED drivers to be controlled by audio synchronization
			1	Enables LED drivers to be controlled through I^2C
PS1	I^2C_LED1	0	0	Disables the LED1 driver, if I^2C_SEL is set
			1	Enables the LED1 driver, if I^2C_SEL is set
PS2	I^2C_LED2	0	0	Disables the LED2 driver, if I^2C_SEL is set
			1	Enables the LED2 driver, if I^2C_SEL is set
PS3	I^2C_LED3	0	0	Disables the LED3 driver, if I^2C_SEL is set
			1	Enables the LED3 driver, if I^2C_SEL is set
PS4	RSVD	0	0	RESERVED
			1	RESERVED

Table 6. Current Select Register

Data Bit	Bit Name	Default Value	Condition	Function	
CSO	ILED1_0	0	0	Programs the current drive of the LED1 driver. Current drive for LED1 is set as follows:	
			1	**ILED1<1:0>**	**Current Drive Setting**
CS1	ILED1_1	1	0	00	0.66X
				01	1X
			1	10	1.33X
				11	2X
CS2	ILED2_0	0	0	Programs the current drive of the LED2 driver. Current drive for LED2 is set as follows:	
			1	**ILED2<1:0>**	**Current Drive Setting**
CS3	ILED2_1	1	0	00	0.66X
				01	1X
			1	10	1.33X
				11	2X

Table 6. Current Select Register (continued)

Data Bit	Bit Name	Default Value	Condition	Function	
CS4	ILED3_0	0	0	Programs the current drive of the LED3 driver. Current drive for LED3 is set as follows:	
			1	**ILED3<1:0>**	**Current Drive Setting**
CS5	ILED3_1	1	0	00	0.66X
				01	1X
			1	10	1.33X
				11	2X

Table 7. Gain Select Register

Data Bit	Bit Name	Default Value	Condition	Function	
GSO	MGAIN0	0	0	Programs the gain response of the midband audio synchronized filter which drives the LED2 PWM color LED driver for the midband audio frequencies. Gain is set as follows:	
			1		
GS1	MGAIN1	1	0	**MGAIN<2:0>**	**Midband Filter Gain**
			1		
GS2	MGAIN2	0	0	000	minimum
			1	001	low
				010	medium
				011	high
				100	maximum
GS3	SGAIN0	0	0	Programs the audio gain of the input summing amplifier. Gain is set as follows:	
			1	**SGAIN<2:0>**	**Input Signal Gain**
GS4	SGAIN1	1	0	000	–11dB
			1	001	–6.5dB
GS5	SGAIN2	0	0	010	0dB
				011	3.5dB
			1	100	6dB
				101	10dB
				110	12dB

I²C COMPATIBLE INTERFACE

The LM4970 uses a serial bus which conforms to the I²C protocol to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector) with a pullup resistor (typically 10kΩ). The maximum clock frequency specified by the I²C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4970.

The I²C address for the LM4970 is determined using the ADR pin. The LM4970's two possible I²C chip addresses are of the form $111101X_10$ (binary), where $X_1 = 0$, if ADR is logic low; and $X_1 = 1$, if ADR is logic high. If the I²C interface is used to address a number of chips in a system, the LM4970's chip address can be changed to avoid any possible address conflicts.

The bus format for the I²C interface is shown in Figure 14. The data is latched in on the rising edge of the clock. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the clock level is high.

After the last bit of the address bit is sent, the master checks for the LM4970's acknowledge. The master releases the data line high (through a pullup resistor). Then the master sends a clock pulse. If the LM4970 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not low, then the master should send a "stop" signal (discussed later) and abort the transfer.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must check for another acknowledge to see if the LM4970 received the data.

If the master has more data bytes to send to the LM4970, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes high while the clock signal is high. The data line should be held high when not in use.

AUDIO SYNCHRONIZATION MODE

The LM4970 features an audio synchronization mode where each PWM color LED driver output is dependent on the audio input signal. The audio synchronization mode allows each LED output to react to the amplitude of the audio input signal, according to the LED output's assigned frequency band. Audio synchronization mode is activated by clearing the I2C_SEL bit in the Pattern Select Register.

The audio synchronization filter separates the mixed audio signal into three frequency bands: lowband, midband, and highband. Each frequency band is assigned to a particular PWM LED output, with lowband controlling the duty cycle of the LED1 output, midband controlling the duty cycle of the LED2 output, and highband controlling the duty cycle of the LED3 output. This occurs whenever the audio synchronization randomizer is not turned on. The operation of the audio synchronization randomizer is explained in the AUDIO SYNCHRONIZATION RANDOMIZER section. The duty cycle of any given LED output is dependent upon the amplitude of the audio signal for its particular frequency band. An increase in the amplitude of the audio signal will increase the duty cycle of the PWM LED driver. LEDs driven with a higher duty cycle results in a brighter lighting effect.

The LM4970 has three single-ended analog audio inputs designated M_{IN}, L_{IN}, and R_{IN}, where mono voice data is routed to M_{IN} and stereo MP3 or stereo FM radio data is routed to L_{IN} and R_{IN}. Audio signals coupled in from M_{IN}, L_{IN}, and R_{IN} are mixed together by an audio input summing amplifier. The gain of the audio input summing amplifier is programmed by the SGAIN<2:0> bits of the Gain Select Register. Increasing the gain of the audio input summing amplifier will increase the intensity of the LEDs in audio synchronization mode.

The pole of the low pass filter band is set by the filter cap, Cfilt, and an internal 4kΩ resistor. The pole of the high pass filter band is internally set by programming the HPF_F<1:0> bits of the Frequency Select Register. The midband frequency band is a function of the lowband and highband poles. The gain response of the midband frequency band can be set by programming the MGAIN<2:0> bits of the Gain Select Register.

To minimize LED leakage between audio bands, care should be taken when selecting input gain, midband gain, Cfilt, and LED current drive. There is a trade off between LED brightness and LED leakage in other audio bands. Leakage can be minimized by reducing LED current drive and input gain. Please refer to the frequency response graphs found in the Typical Performance Characteristics section as a guideline to minimize LED leakage.

AUDIO SYNCHRONIZATION RANDOMIZER

The LM4970 features a randomizer block that randomizes the frequency band assigned to each PWM LED driver during audio synchronization operation. The randomizer is activated by setting the RAND bit in the Mode Select Register. Clearing the RAND bit will disable the randomizer. The randomizer can only be activated when the LM4970 is programmed to audio synchronization mode. The interval at which randomizer assigns a new frequency band is set to occur once every 3.2 seconds. The randomizer ensures that all the colored LEDs will light up over a long duration even if the audio input has a fixed frequency.

I²C PATTERN MODE

The LM4970 features an I²C pattern mode for applications where direct control of the LED outputs is required. I²C pattern mode is activated by setting the I2C_SEL bit in the Pattern Select Register. The LED1 output duty cycle can be programmed to 100% by setting the I2C_LED1 bit in the Pattern Select Register. Clearing the I2C_LED1 bit sets the LED1 output duty cycle to 0%. The LED2 output duty cycle can be programmed to 100% by setting the I2C_LED2 bit in the Pattern Select Register. Clearing the I2C_LED2 bit sets the LED2 output duty cycle to 0%. The LED3 output duty cycle can be programmed to 100% by setting the I2C_LED3 bit in the Pattern Select Register. Clearing the I2C_LED3 bit sets the LED3 output duty cycle to 0%. Color LEDs driven at 100% duty cycle are fully on, and driven at 0% duty cycle are fully off.

PWM FREQUENCY

The PWM frequency of the color LED drivers is programmed through the PWM_F<1:0> bits of the Frequency Select Register. The LM4970 features four different PWM frequency settings: 15kHz, 60Hz, 7Hz, and 4Hz. PWM frequency is analogous to the sampling rate of the audio input signal. A higher PWM frequency setting will result in a more accurate LED representation of the audio input signal in the audio synchronization mode. However, a PWM frequency that is set too high will decrease the ON time of the LED which will result in reduced LED intensity. A PWM frequency setting of 60Hz results in an optimal balance between LED accuracy and intensity.

DRIVING RGB LED MODULES

The LM4970's PWM LED outputs can be used to drive individual color LEDs or RGB LED modules. When driving RGB LED modules in audio synchronization mode, the color and intensity of the RGB LED module will be dependent on the audio input signal. In I²C pattern mode, the RGB LED module can be set to any of seven distinct colors, based on the status of the I2C_LED1, I2C_LED2, and I2C_LED3 bit settings.

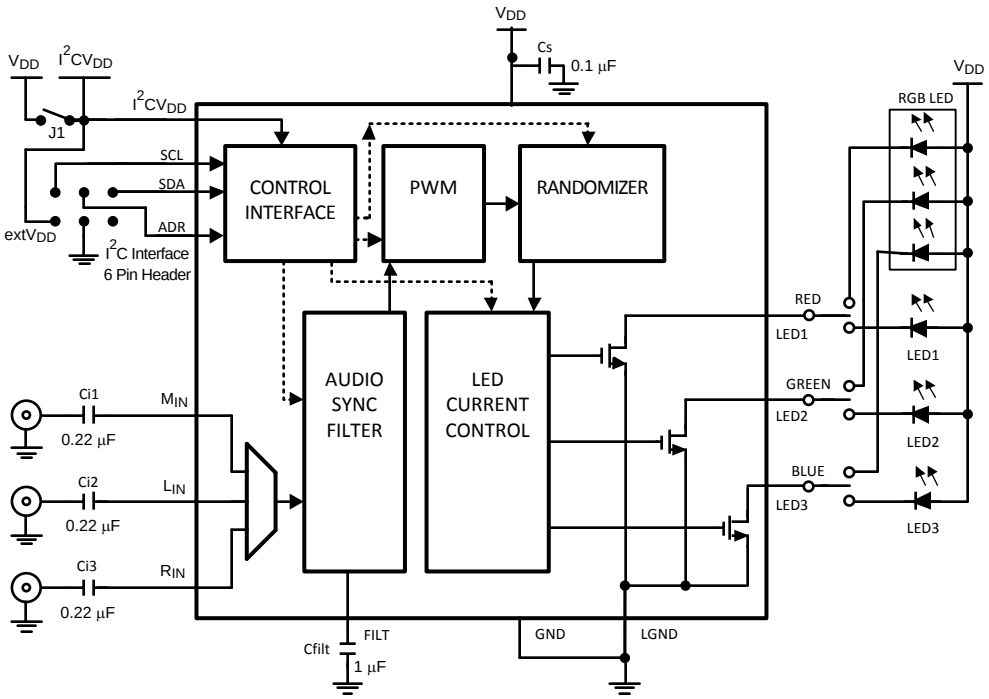


Figure 15. Reference Design Board Schematic

Demonstration Board NHK PCB Layout

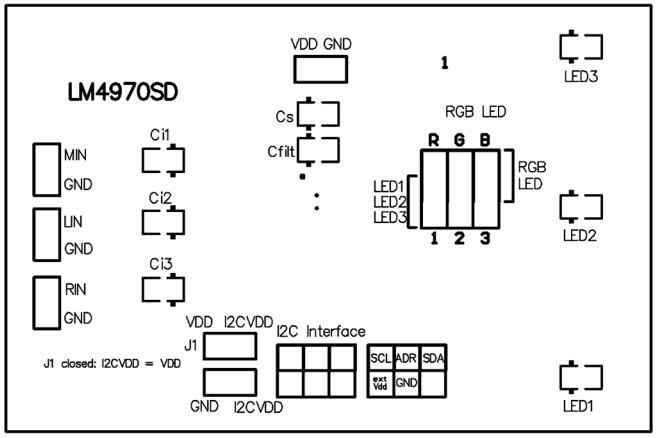


Figure 16. Recommended NHK PCB Layout: Top Silkscreen

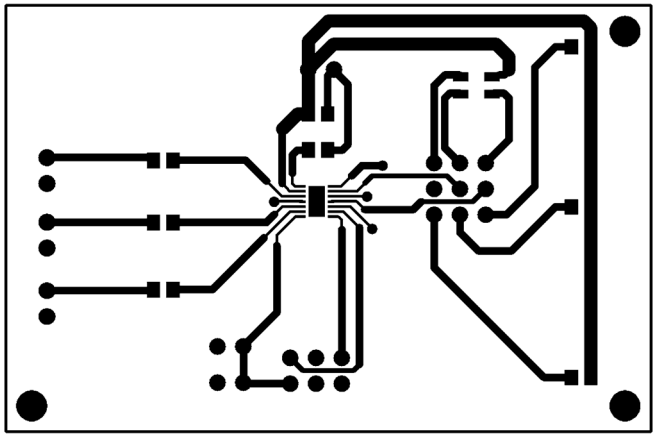


Figure 17. Recommended NHK PCB Layout: Top Layer

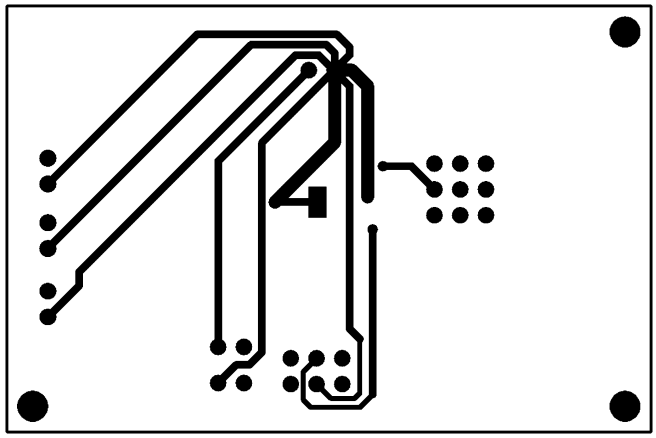


Figure 18. Recommended NHK PCB Layout: Bottom Layer

Revision History

Rev	Date	Description
1.1	5/26/06	On Table 2 (pg 8), col D7 for Pattern Select, changed the '1' into '0'.
1.2	04/01/08	Added the last paragraph under the AUDIO SYNCHRONIZATION MODE.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4970SD/NOPB	ACTIVE	WSON	NHK	14	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L4970	Samples
LM4970SDX/NOPB	ACTIVE	WSON	NHK	14	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L4970	Samples

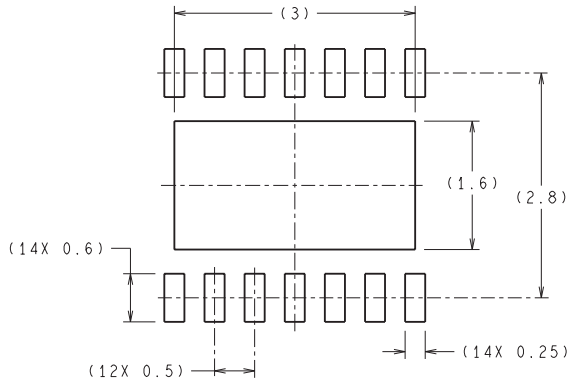
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

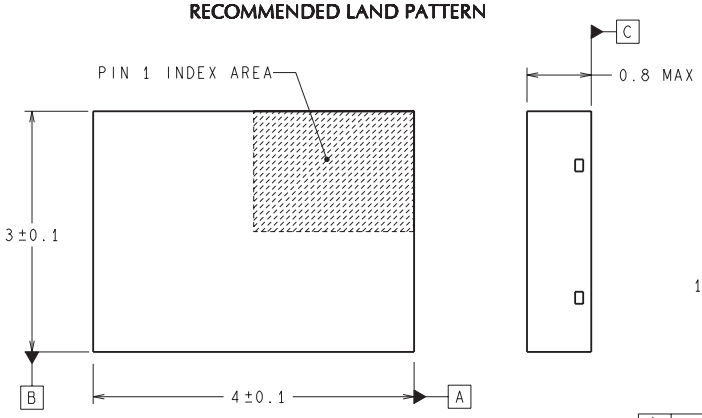
(4) Only one of markings shown within the brackets will appear on the physical device.

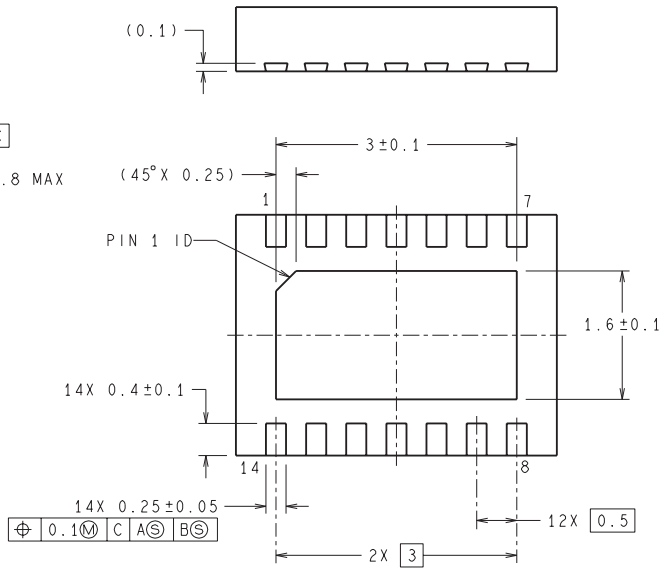
NHK0014A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





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