National Semiconductor

LM607/LM607A/LM607B Precision Operational Amplifier

General Description

The LM607 series of precision operational amplifiers are trimmed at wafer sort to extremely low values of offset voltage. Advanced circuit design and testing techniques allow guaranteed drift specifications as low as 0.3 μV/°C with offsets as low as 25 μV.

Other input parameters are equally impressive. The typical open loop voltage gain of 5 Million yields extremely low error in high-gain applications. CMRR and PSRR are typically 140 dB.

Using Super-Beta transistors in the front end enables the LM607 to operate at high input stage current while maintaining low values of input bias current (1 nA typ.) This gives the part its low input voltage noise: 6.5 nV/√Hz.

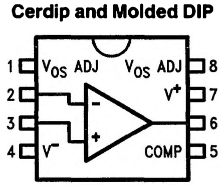
High operating currents also help give the LM607 its high gain-bandwidth product of 1.8 MHz and slew rate of 0.7V/μs. Despite its higher speed, the LM607 draws less supply current than OP-07 and OP-77 types: only 1 mA at ±15V supplies.

Features

- Low V_{OS} LM607A: 25 μV max
- Low drift LM607A: 0.3 μV/°C max
- Drift *100% tested:* A and B grades
- High gain LM607A: 5 million min
- High CMRR LM607A: 124 dB min
- High PSRR LM607A: 120 dB min
- Low noise 6.5 nV/√Hz @ 1 kHz, 7.2 nV/√Hz @ 10 Hz
- High speed 1.8 MHz gain-bandwidth, 0.7V/μs slew rate
- Low supply current 1 mA
- Wide input common mode range ±13.5V
- Wide supply range ±3V to ±18V
- Overcompensation Allows driving high C_L

Connection Diagrams

Cerdip and Molded DIP



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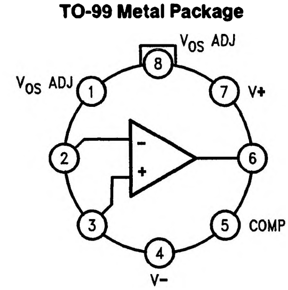
Top View

TO-99 Metal Package



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Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military	Commercial	
TO-99	LM607AMH LM607BMH	LM607ACH LM607BCH LM607CH	H08C
8-Pin Cerdip	LM607AMJ LM607BMJ	LM607ACJ LM607BCJ LM607CJ	J08A
8-Pin Molded DIP		LM607ACN LM607BCN LM607CN	N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Overdrive Current (Note 7)	±25 mA
Supply Voltage	44V
Input Voltage	Supply Voltage
Output Short Circuit to Gnd	Continuous
Power Dissipation (Note 9)	500 mW
Maximum Junction Temperture	150°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD Tolerance C_{ZAP} = 100 pF, R_{ZAP} = 1.5 kΩ	2000V

Operating Rating

Temperature Range (Note 9)

LM607AM/LM607BM	$-55°C \le T_J \le +125°C$
LM607C/LM607AC/LM607BC	$0°C \le T_J \le +70°C$

Electrical Characteristics

All limits guaranteed for T_J = 25°C, V_{CM} = 0, V_O = 0, and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM607AM Tested Limit (Note 5)	LM607AM Design Limit (Note 6)	LM607BM Tested Limit (Note 5)	LM607BM Design Limit (Note 6)	Units
Input Offset Voltage	(Note 2)	15	25 **80**		60 **120**		μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.3**		**0.6**		μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2					μV/mo Max
Input Bias Current		1	2 **4**		3 **6**		nA Max
Input Offset Current		0.5	2 **4**		2.8 **5.6**		nA Max
Input Noise Voltage	0.1 to 10 Hz	0.2		0.5		0.5	μV p-p Max
Input Noise Voltage Density	f = 10 Hz f = 100 Hz f = 1 kHz	7.2 6.6 6.5	18 8	 10 	18 8	 10 	nV/√Hz Max
Input Noise Current	0.1 to 10 Hz	14					pA p-p Max
Input Noise Current Density	f = 10 Hz f = 100 Hz f = 1 kHz	0.32 0.14 0.12					pA/√Hz Max
Input Resistance	Differential Mode Common Mode	2 100					MΩ GΩ
Input Voltage Range		±13.5	±13 **±12.5**		±13 **±12.5**		V Min
Common-Mode Rejection Ratio	V_{CM} = ±13V **V_{CM} = ±12.5V**	140	124 **120**		116 **112**		dB Min
Power Supply Rejection Ratio	V_S = ±3V to ±18V (Note 8)	140	120 **117**		114 **112**		dB Min
Large-Signal Voltage Gain	V_O = ±10V $R_L \ge 2$ kΩ $R_L \ge 1$ kΩ	 10000 5000	 5000 **2000** 1500		 2000 **1500** 1000		V/mV Min

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM607AM		LM607BM		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Output Voltage Swing	$R_L \geq 2\ k\Omega$ $R_L \geq 1\ k\Omega$	±13.8	±13 **±12.5** ±12.5		±13 **±12.5** ±12.5		V Min
Slew Rate		0.7		0.4		0.4	V/μs Min
Gain-Bandwidth Product	f = 100 kHz	1.8		1.0		1.0	MHz Min
Open-Loop Output Resistance		50					Ω
Supply Current		1	1.5 **2.0**		1.5 **2.0**		mA Max
Offset Adjust Range		1.5					mV

Electrical Characteristics

All limits guaranteed for $T_J = 25°C$, $V_{CM} = 0$, $V_O = 0$, and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM607AC		LM607BC		LM607C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Input Offset Voltage	(Note 2)	15	25 **40**		60 **90**		150	**250**	μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.3**		**0.6**			**2.5**	μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2							μV/mo Max
Input Bias Current		1	2	**4**	3	**6**	10	**14**	nA Max
Input Offset Current		0.5	2	**4**	2.8	**5.6**	6	**10**	nA Max
Input Noise Voltage	0.1 to 10 Hz	0.2		0.5		0.5		0.5	μV p-p Max
Input Voltage Noise Density	f = 10 Hz f = 100 Hz f = 1 kHz	7.2 6.6 6.5	18 8	 10 	18 8	 10 	20 11.5	 13.5 	$nV/\sqrt{Hz}$ Max
Input Noise Current	0.1 to 10 Hz	14							pA p-p Max
Input Noise Current Density	f = 10 Hz f = 100 Hz f = 1 kHz	0.32 0.14 0.12							$pA/\sqrt{Hz}$ Max
Input Resistance	Differential Mode Common Mode	2 100							MΩ GΩ
Input Voltage Range		±13.5	±13	**±12.5**	±13	**±12.5**	±13	**±12.5**	V Min
Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$ $\mathbf{V_{CM} = \pm 12.5\ V}$	140	124	**120**	116	**112**	110	**108**	dB Min
Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$ (Note 8)	140	120	**117**	114	**112**	110	**108**	dB Min

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM607AC		LM607BC		LM607C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Large-Signal Voltage Gain	$V_O = \pm 10V$ $R_L \geq 2\ k\Omega$ $R_L \geq 1\ k\Omega$	10000 5000	5000 1500	**2000**	2000 1000	**1500**	1500 1000	**1000**	V/mV Min
Output Voltage Swing	$R_L \geq 2\ k\Omega$ $R_L \geq 1\ k\Omega$	±13.8	±13 ±12.5	**±12.5**	±13 ±12.5	**±12.5**	±12.5 ±12	**±12**	V Min
Slew Rate		0.7		0.4		0.4		0.4	V/μs Min
Gain-Bandwidth Product	f = 100 kHz	1.8		1.0		1.0		1.0	MHz Min
Open-Loop Output Resistance		50							Ω
Supply Current		1	1.5	**2.0**	1.5	**2.0**	1.8	**2.2**	mA Max
Offset Adjust Range		1.5							mV

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Input offset voltage for A and B grades is tested and guaranteed with the device fully warmed up. See *Figure 1* in the Application Hints for test circuit. Warmup drift is typically 3 μV settling out in 5 minutes. The LM607C offset voltage is measured by automated test equipment within 200 ms of applying power.

Note 3: Input offset voltage drift is defined as $[V_{OS}(70°C) - V_{OS}(-5°C)]/75°C$ for the commercial temperature range. For the military temperature range, the input offset voltage drift is measured from room temperature to both extremes: both $[V_{OS}(25°C) - V_{OS}(-55°C)]/80°C$ and $[V_{OS}(125°C) - V_{OS}(25°C)]/100°C$.

Note 4: Input offset voltage long term stability refers to the average trend line of V_{OS} vs. time over extended periods of time after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2 μV.

Note 5: Guaranteed and 100% production tested.

Note 6: Limits at temperature extremes are guaranteed via correlation using Standard Statistical Quality Control (SQC) Methods. All limits are to be used to calculate Average Outgoing Quality Level (AOQL).

Note 7: Inputs are protected by back-to-back diodes to prevent zener breakdown of the input transistors. Series limiting resistors have not been included since they degrade noise performance. Excessive current may flow if a differential voltage in excess of 0.7V is applied.

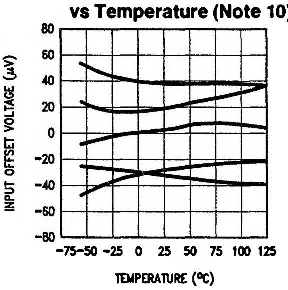
Note 8: Power Supply Rejection Ratio is tested by moving both power supplies together from their minimum to maximum values.

Note 9: Typical thermal resistance of the molded package is 95°C/W junction-to-ambient. Typical thermal resistance of the metal can package is 150°C/W junction-to-ambient and 17°C/W junction-to-case.

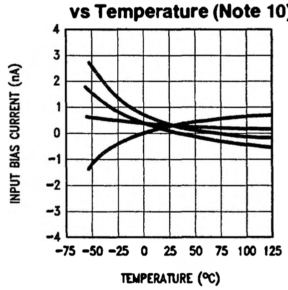
Note 10: These units selected to illustrate the type of variations that may be encountered. (This note refers to particular curves within the Typical Performance Characteristics.)

Typical Performance Characteristics $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 2k$ unless otherwise indicated

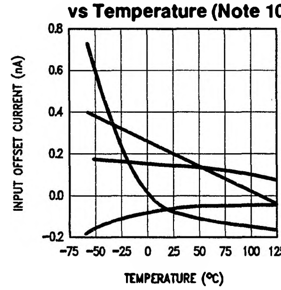
Input Offset Voltage of 5 Representative Units vs Temperature (Note 10)



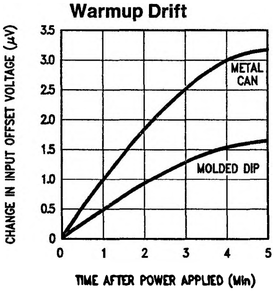
Input Bias Current of 4 Representative Units vs Temperature (Note 10)



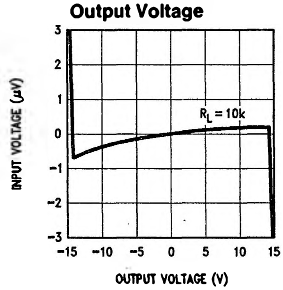
Input Offset Current of 4 Representative Units vs Temperature (Note 10)



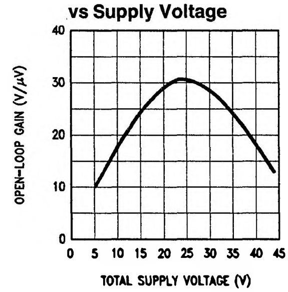
Warmup Drift



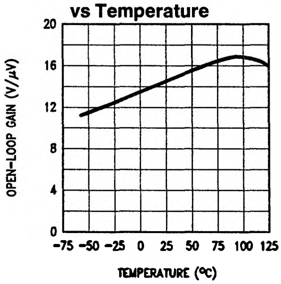
Input Voltage vs Output Voltage



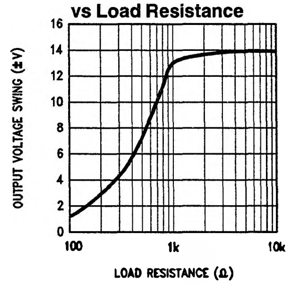
Open-Loop Gain vs Supply Voltage



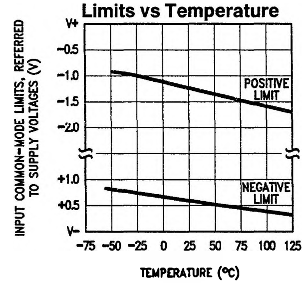
Open-Loop Gain vs Temperature



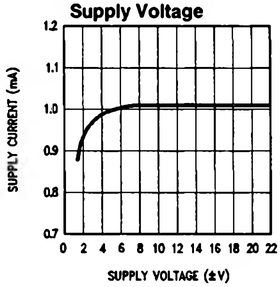
Output Voltage Swing vs Load Resistance



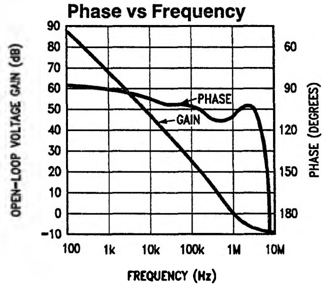
Input Common-Mode Limits vs Temperature



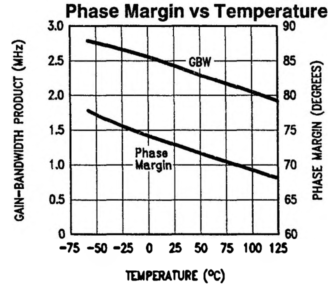
Supply Current vs Supply Voltage



Open Loop Gain and Phase vs Frequency



Gain-Bandwidth Product, Phase Margin vs Temperature



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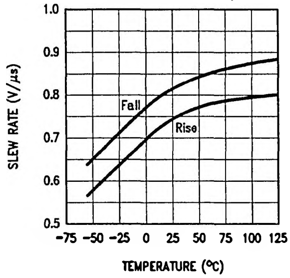
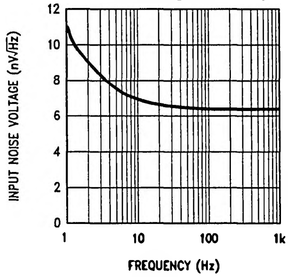
Typical Performance Characteristics (Continued)

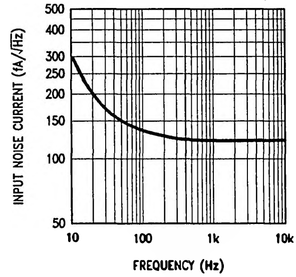
Slew Rate vs Temperature



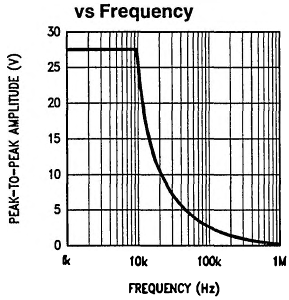
Noise Voltage vs Frequency



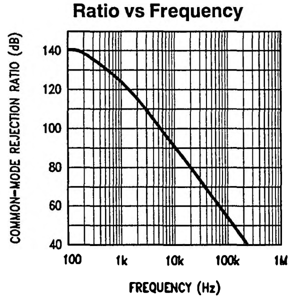
Noise Current vs Frequency



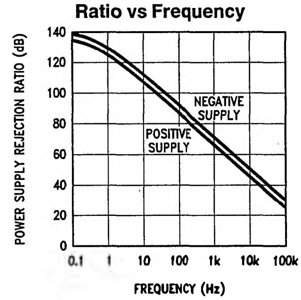
Maximum Output Swing vs Frequency



Common-Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency



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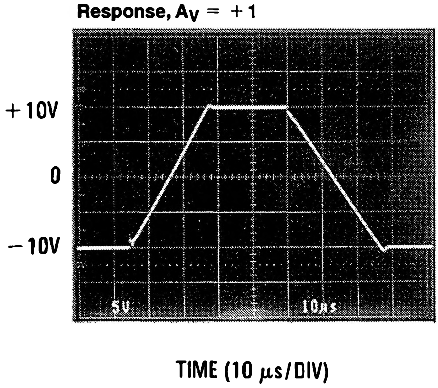
Large-Signal Pulse Response, $A_V = +1$



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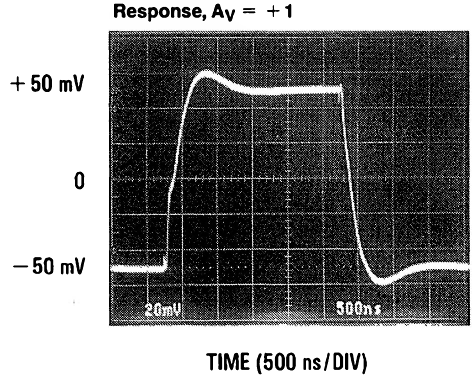
Small-Signal Pulse Response, $A_V = +1$



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Application Hints

OFFSET VOLTAGE

Offset voltage of the LM607 is internally trimmed to a very low value. The data sheet V_{OS} specification applies at T_J = 25°C, V_{CM} = 0 and ±15V supplies. For other conditions, temperature drift, common-mode rejection and power-supply rejection errors must be taken into account.

Although the LM607C is specified as T_J = 25°C, the 3 μV typical warmup drift is a small fraction of its 100 μV max offset. For the 25 μV LM607A and 50 μV LM607B grades, the offset voltage is measured fully warmed up with the circuit of *Figure 1* approximately 5 minutes after applying power.

To measure V_{OS} with high accuracy, gain must be taken right at the device as shown, otherwise the offset voltage would get swamped out by noise and thermoelectric voltages. Thermocouples occur in the devices, the IC socket and the resistor across the device inputs (R2), all of which must be held isothermal. Usually best results are obtained by placing the circuit in a box or chamber to minimized airflow and employing a long thermal soak time. R2 should be mounted symmetrically with respect to potential thermal gradients: e.g. *not* perpendicular to the board but instead parallel to the board and the device socket. In addition, R2 should have low thermal EMF. Cermet or nichrome metal film types are acceptable; avoid tin-oxide resistors.

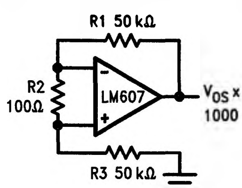

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FIGURE 1. Offset Voltage Test Circuit

OFFSET NULLING

This is usually not required on the LM607 family since its offset voltage is internally trimmed. An offset adjust range of approximately ±1.5 mV is available using a single 10 or 20 kΩ potentiometer as shown in *Figure 2.* With these values, the adjustment is relatively linear over the entire range. If a 100 kΩ potentiometer is used, the adjustment becomes very coarse at the extremes (above 700 μV) but fine in the center, which makes it easier to precisely null the offset. For even more sensitivity, employ a pot in conjunction with two fixed resistors. For example the circuit of *Figure 3* has an adjustment range of ±150 μV.

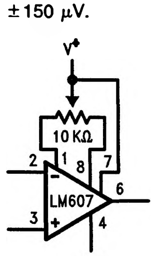

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FIGURE 2. Offset Adjust Circuit

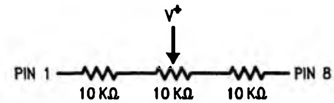

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FIGURE 3. Improved Sensitivity Offset Adjust

Because adjusting the offset voltage of an LM607 will alter its offset voltage temperature drift, caution is advised. Every 100 μV of offset will produce a 0.33 μV/°C drift component. For this reason the offset adjust potentiometer should not be used to null out a sensor offset if system temperature drift is important; rather a stable voltage reference must be added to the sensor voltage. Offset voltage drift is guaranteed by design for the LM607C either with or without external nulling. The higher precision A and B grades are 100% drift tested and guaranteed without nulling only.

OVERCOMPENSATION

Without any external compensation, the LM607 is stable at unity gain and up to 750 pF load capacitance. It has a slew rate of 0.7V/μs and a gain-bandwidth product of 1.8 MHz. If desired, the amplifier may be overcompensated by adding external components as shown in *Figure 4*. This increases maximum capacitive loading to 0.01 μF while decreasing slew rate to 0.13V/μs and bandwidth to 200 kHz. If overcompensation is not desired, pin 5 should be left open.

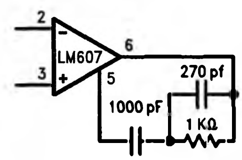

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FIGURE 4. Overcompensation

NOISE

The LM607 achieves lower voltage noise than the OP-07 primarily by operating at higher input stage current. Its superbeta input transistors and trimmed bias-current compensation prevent the bias current from increasing. When measuring spot noise, a circuit as shown in *Figure 5* is recommended. The DUT runs at a gain of 100 will not roll off until approximately 15 kHz. Another gain of 100 amplifier following brings total DUT-input-referred gain up to 10,000 to minimize sensitivity to EMI in the environment. When measuring spot noise at 100 Hz, it is recommended that the bandwidth be 20 Hz or less to minimize pickup of 120 Hz, the second harmonic of line frequency.

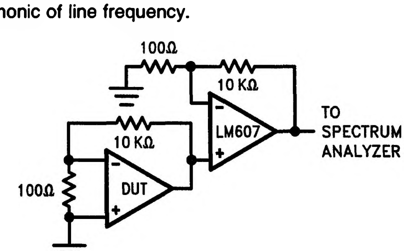

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FIGURE 5. Spot Noise Test Circuit

Application Hints (Continued)

The circuit used to measure peak-to-peak noise in the 0.1 to 10 Hz range is shown in *Figure 6*. The device should be warmed up for about 2 minutes and shielded from air currents to minimize warmup drift and thermoelectric voltages. The test time should be limited to only 10 seconds, as this limits noise contributions below 0.1 Hz, in addition to the single zero rolloff. The measuring equipment must be flat beyond this bandwidth. DC coupling must be employed to ensure this. Certain types of X-Y plotters may not be usable because of severe rolloff above a few Hz.

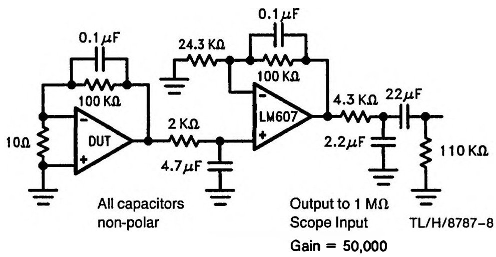

FIGURE 6. 0.1 to 10 Hz Noise Test Circuit

Input Overdrive

The LM607's input-protection diodes prevent zener breakdown of the input transistors and the ensuing degradation of input DC parameters. Current limiting resistors have not been included as they would degrade input noise voltage. Input current should be limited to ±25 mA to avoid potential damage to the IC metallization.

In voltage follower applications, large input voltage steps may be coupled directly to the op amp's output via the protection diodes. If the input and feedback resistances are low in value, the output stage may be driven temporarily into current limit. The resulting output waveform exhibits an initial fast step when the diodes are conducting followed by a slight glitch as the amplifier comes out of current limit before true slewing is observed. For best results, use input and feedback resistors of 2 kΩ each in parallel with 30 pF capacitors. The capacitors eliminate input and feedback poles which respectively cause signal rolloff and instabilities.