

## LMC6035/LMC6036 Low Power 2.7V Single Supply CMOS Operational Amplifiers

Check for Samples: [LMC6035](#), [LMC6036](#)

### FEATURES

- (Typical Unless Otherwise Noted)
- LMC6035 in DSBGA Package
- Guaranteed 2.7V, 3V, 5V and 15V Performance
- Specified for 2 k $\Omega$  and 600 $\Omega$  Loads
- Wide Operating Range: 2.0V to 15.5V
- Ultra Low Input Current: 20fA
- Rail-to-Rail Output Swing
  - @ 600 $\Omega$ : 200mV from Either Rail at 2.7V
  - @ 100k $\Omega$ : 5mV from Either Rail at 2.7V
- High Voltage Gain: 126dB
- Wide Input Common-Mode Voltage Range
  - -0.1V to 2.3V at  $V_S = 2.7V$
- Low Distortion: 0.01% at 10kHz
- LMC6035 Dual LMC6036 Quad
- See AN-1112 for DSBGA Considerations

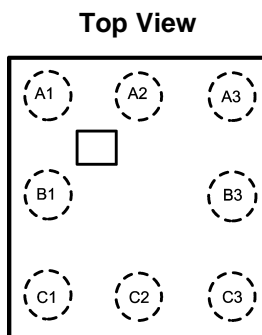
### DESCRIPTION

The LMC6035/6 is an economical, low voltage op amp capable of rail-to-rail output swing into loads of 600 $\Omega$ . LMC6035 is available in a chip sized package (8-Bump DSBGA) using micro SMD package technology. Both allow for single supply operation and are guaranteed for 2.7V, 3V, 5V and 15V supply voltage. The 2.7 supply voltage corresponds to the End-of-Life voltage (0.9V/cell) for three NiCd or NiMH batteries in series, making the LMC6035/6 well suited for portable and rechargeable systems. It also features a well behaved decrease in its specifications at supply voltages below its guaranteed 2.7V operation. This provides a “comfort zone” for adequate operation at voltages significantly below 2.7V. Its ultra low input currents ( $I_{IN}$ ) makes it well suited for low power active filter application, because it allows the use of higher resistor values and lower capacitor values. In addition, the drive capability of the LMC6035/6 gives these op amps a broad range of applications for low voltage systems.

### APPLICATIONS

- Filters
- High Impedance Buffer or Preamplifier
- Battery Powered Electronics
- Medical Instrumentation

### Connection Diagram



**Figure 1. 8-Bump DSBGA Package  
(Bump Side Down)  
See Package Number YZR0008**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

**Table 1. DSBGA Connection Table**

Bump Number	LM6035IBP LMC6035IBPX	LMC6035ITL LMC6035ITLX
A1	OUTPUT A	OUTPUT B
B1	IN A <sup>-</sup>	V <sup>+</sup>
C1	IN A <sup>+</sup>	OUTPUT A
C2	V <sup>-</sup>	IN A <sup>-</sup>
C3	IN B <sup>+</sup>	IN A <sup>+</sup>
B3	IN B <sup>-</sup>	V <sup>-</sup>
A3	OUTPUT B	IN B <sup>+</sup>
A2	V <sup>+</sup>	IN B <sup>-</sup>



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings** <sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	Human Body Model	3000V
	Machine Model	300V
Differential Input Voltage		± Supply Voltage
Supply Voltage (V <sup>+</sup> – V <sup>-</sup> )		16V
Output Short Circuit to V <sup>+</sup>		See <sup>(4)</sup>
Output Short Circuit to V <sup>-</sup>		See <sup>(5)</sup>
Lead Temperature (soldering, 10 sec.)		260°C
Current at Output Pin		±18mA
Current at Input Pin		±5mA
Current at Power Supply Pin		35mA
Storage Temperature Range		-65°C to +150°C
Junction Temperature <sup>(6)</sup>		150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) Human body model, 1.5kΩ in series with 100pF.
- (4) Do not short circuit output to V<sup>+</sup> when V<sup>+</sup> is greater than 13V or reliability will be adversely affected.
- (5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 30mA over long term may adversely affect reliability.
- (6) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> – T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC board with no air flow.

**Operating Ratings** <sup>(1)</sup>

Supply Voltage		2.0V to 15.5V
Temperature Range	LMC6035I and LMC6036I	-40°C ≤ T <sub>J</sub> ≤ +85°C
Thermal Resistance (θ <sub>JA</sub> )	8-pin VSSOP	230°C/W
	8-pin SOIC	175°C/W
	14-pin SOIC	127°C/W
	14-pin TSSOP	137°C/W
	8-Bump (6 mil) DSBGA	220°C/W
	8-Bump (12 mil) Thin DSBGA	220°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

## DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		LMC6035I/LMC6036I			Units
				Min (1)	Typ (2)	Max (1)	
$V_{\text{OS}}$	Input Offset Voltage				0.5	5 <b>6</b>	mV
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift				2.3		$\mu\text{V}/^\circ\text{C}$
$I_{\text{IN}}$	Input Current	See (3)			0.02	<b>90</b>	pA
$I_{\text{OS}}$	Input Offset Current	See (3)			0.01	<b>45</b>	PA
$R_{\text{IN}}$	Input Resistance				> 10		Tera $\Omega$
CMRR	Common Mode Rejection Ratio	$0.7\text{V} \leq V_{\text{CM}} \leq 12.7\text{V}$ , $V^+ = 15\text{V}$		63 <b>60</b>	96		dB
+PSRR	Positive Power Supply Rejection Ratio	$5\text{V} \leq V^+ \leq 15\text{V}$ , $V_O = 2.5\text{V}$		63 <b>60</b>	93		dB
–PSRR	Negative Power Supply Rejection Ratio	$0\text{V} \leq V^- \leq -10\text{V}$ , $V_O = 2.5\text{V}$ , $V^+ = 5\text{V}$		74 <b>70</b>	97		dB
$V_{\text{CM}}$	Input Common-Mode Voltage Range	$V^+ = 2.7\text{V}$ For CMRR $\geq 40\text{dB}$			–0.1	0.3 <b>0.5</b>	V
				2.0 <b>1.7</b>	2.3		
		$V^+ = 3\text{V}$ For CMRR $\geq 40\text{dB}$			–0.3	0.1 <b>0.3</b>	V
				2.3 <b>2.0</b>	2.6		
		$V^+ = 5\text{V}$ For CMRR $\geq 50\text{dB}$			–0.5	–0.2 <b>0.0</b>	V
				4.2 <b>3.9</b>	4.5		
		$V^+ = 15\text{V}$ For CMRR $\geq 50\text{dB}$			–0.5	–0.2 <b>0.0</b>	V
				14.0 <b>13.7</b>	14.4		
$A_V$	Large Signal Voltage Gain (4)	$R_L = 600\Omega$	Sourcing	100 <b>75</b>	1000		V/mV
			Sinking	25 <b>20</b>	250		V/mV
		$R_L = 2\text{k}\Omega$	Sourcing		2000		V/mV
			Sinking		500		V/mV

(1) All limits are guaranteed by testing or statistical analysis.

(2) Typical Values represent the most likely parametric norm or one sigma value.

(3) Guaranteed by design.

(4)  $V^+ = 15\text{V}$ ,  $V_{\text{CM}} = 7.5\text{V}$  and  $R_L$  connected to  $7.5\text{V}$ . For Sourcing tests,  $7.5\text{V} \leq V_O \leq 11.5\text{V}$ . For Sinking tests,  $3.5\text{V} \leq V_O \leq 7.5\text{V}$ .

## DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		LMC6035/LMC6036I			Units
				Min (1)	Typ (2)	Max (1)	
$V_O$	Output Swing	$V^+ = 2.7\text{V}$ $R_L = 600\Omega$ to $1.35\text{V}$		2.0 <b>1.8</b>	2.5		V
					0.2	0.5 <b>0.7</b>	
		$V^+ = 2.7\text{V}$ $R_L = 2\text{k}\Omega$ to $1.35\text{V}$		2.4 <b>2.2</b>	2.62		V
					0.07	0.2 <b>0.4</b>	
		$V^+ = 15\text{V}$ $R_L = 600\Omega$ to $7.5\text{V}$		13.5 <b>13.0</b>	14.5		V
					0.36	1.25 <b>1.50</b>	
		$V^+ = 15\text{V}$ , $R_L = 2\text{ k}\Omega$ to $7.5\text{V}$		14.2 <b>13.5</b>	14.8		V
					0.12	0.4 <b>0.5</b>	
$I_O$	Output Current	$V_O = 0\text{V}$	Sourcing	4 <b>3</b>	8		mA
		$V_O = 2.7\text{V}$	Sinking	3 <b>2</b>	5		
$I_S$	Supply Current	LMC6035 for Both Amplifiers $V_O = 1.35\text{V}$			0.65	1.6 <b>1.9</b>	mA
		LMC6036 for All Four Amplifiers $V_O = 1.35\text{V}$			1.3	2.7 <b>3.0</b>	

## AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ <sup>(1)</sup>	Units
SR	Slew Rate	See <sup>(2)</sup>	1.5	V/ $\mu\text{s}$
GBW	Gain Bandwidth Product	$V^+ = 15\text{V}$	1.4	MHz
$\theta_m$	Phase Margin		48	°
$G_m$	Gain Margin		17	dB
	Amp-to-Amp Isolation	See <sup>(3)</sup>	130	dB
$e_n$	Input-Referred Voltage Noise	$f = 1\text{kHz}$ $V_{\text{CM}} = 1\text{V}$	27	nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Referred Current Noise	$f = 1\text{kHz}$	0.2	fA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 10\text{kHz}$ , $A_V = -10$ $R_L = 2\text{k}\Omega$ , $V_O = 8\text{ V}_{\text{PP}}$ $V^+ = 10\text{V}$	0.01	%

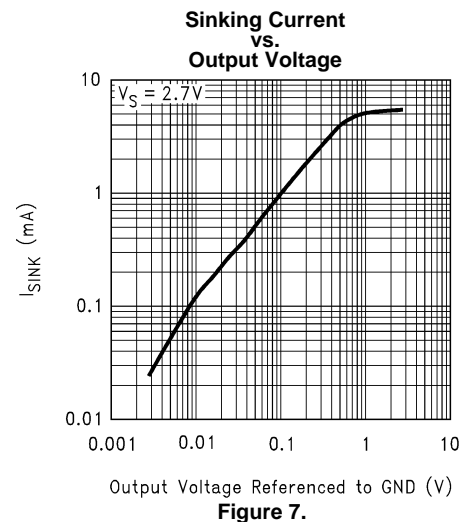
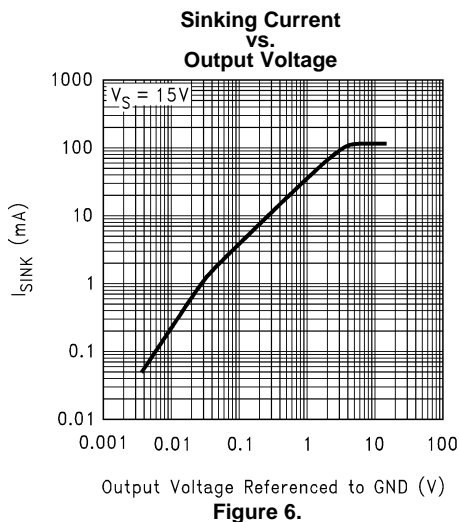
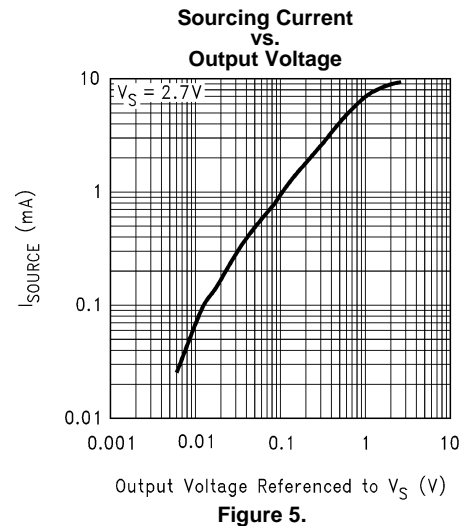
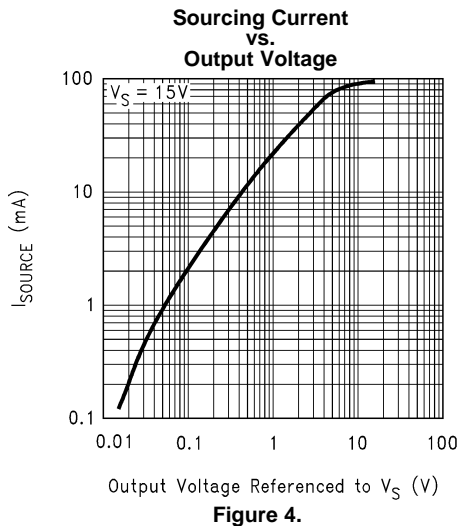
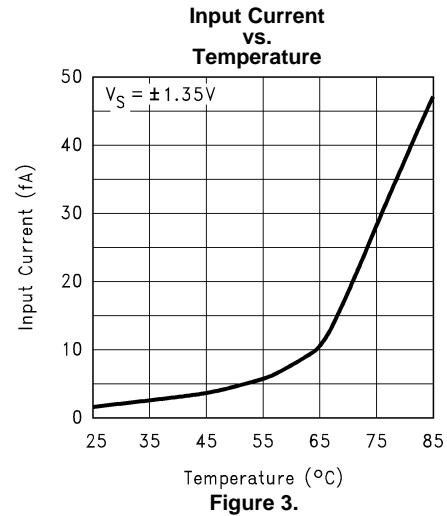
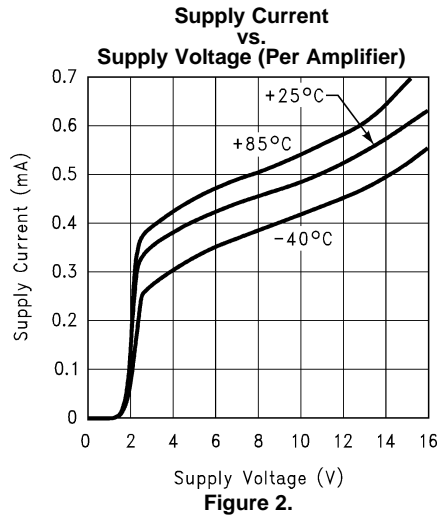
(1) Typical Values represent the most likely parametric norm or one sigma value.

(2)  $V^+ = 15\text{V}$ . Connected as voltage follower with  $10\text{V}$  step input. Number specified is the slower of the positive and negative slew rates.

(3) Input referred,  $V^+ = 15\text{V}$  and  $R_L = 100\text{k}\Omega$  connected to  $7.5\text{V}$ . Each amp excited in turn with  $1\text{kHz}$  to produce  $V_O = 12\text{ V}_{\text{PP}}$ .

## Typical Performance Characteristics

Unless otherwise specified,  $V_S = 2.7V$ , single supply,  $T_A = 25^\circ C$



## Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = 2.7V$ , single supply,  $T_A = 25^\circ C$

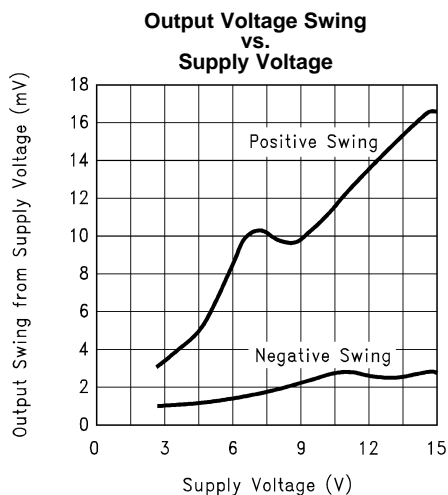


Figure 8.

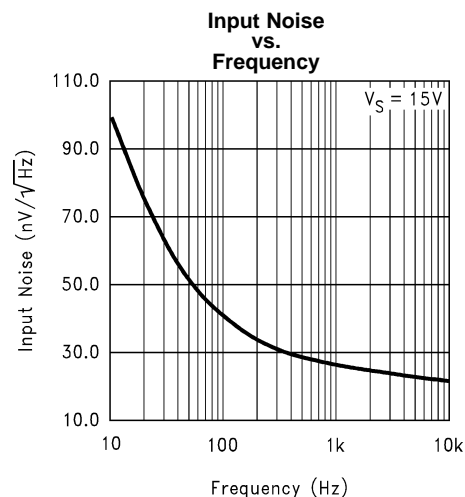


Figure 9.

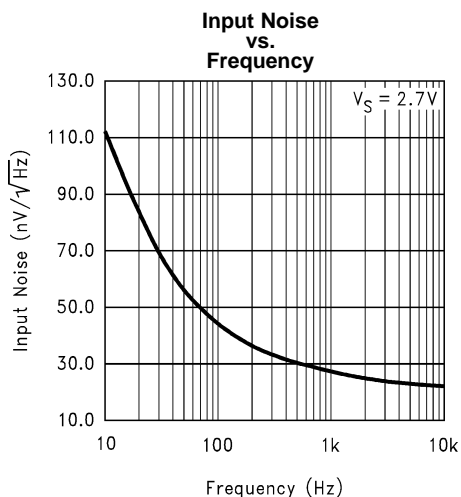


Figure 10.

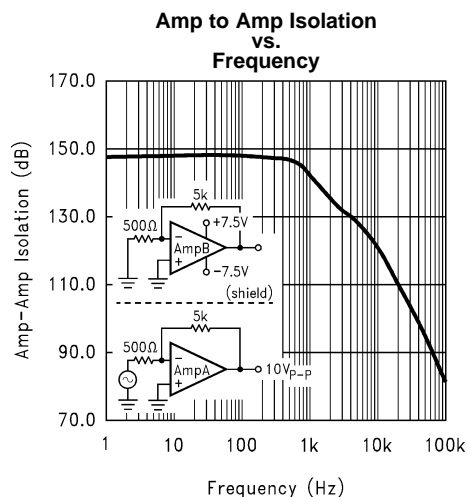


Figure 11.

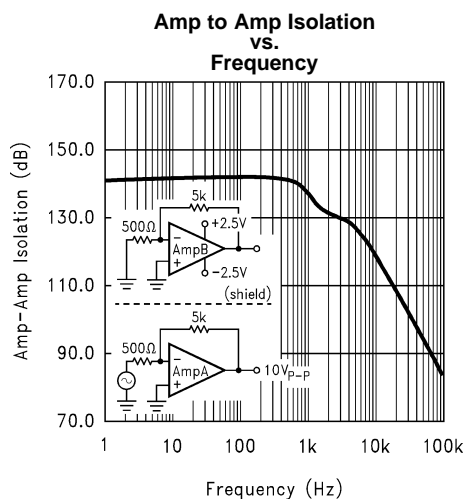


Figure 12.

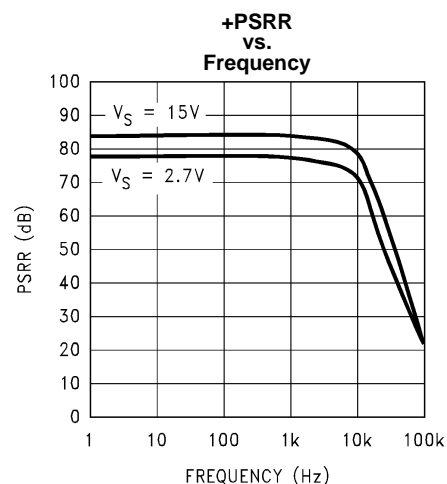


Figure 13.

## Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = 2.7V$ , single supply,  $T_A = 25^\circ C$

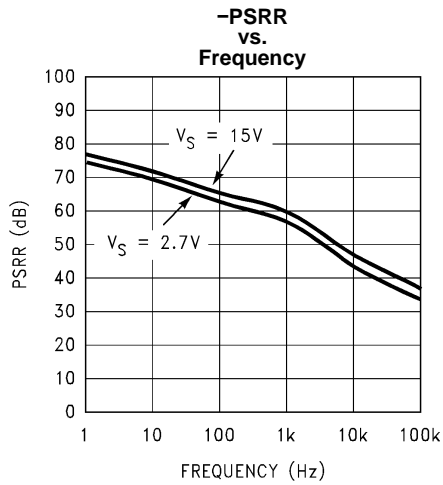


Figure 14.

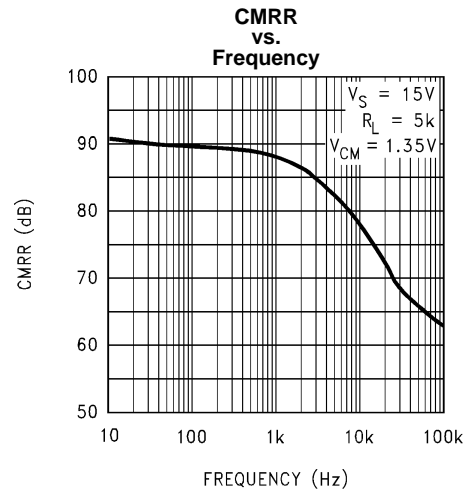


Figure 15.

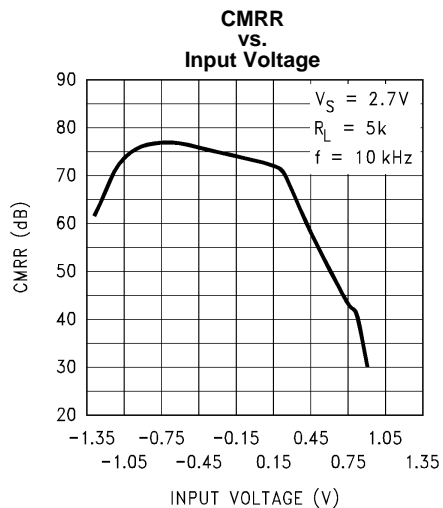


Figure 16.

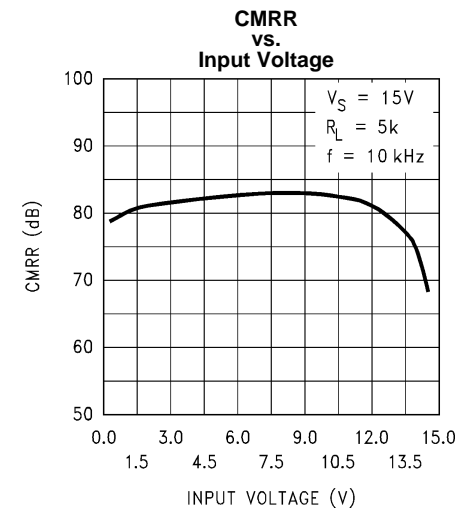


Figure 17.

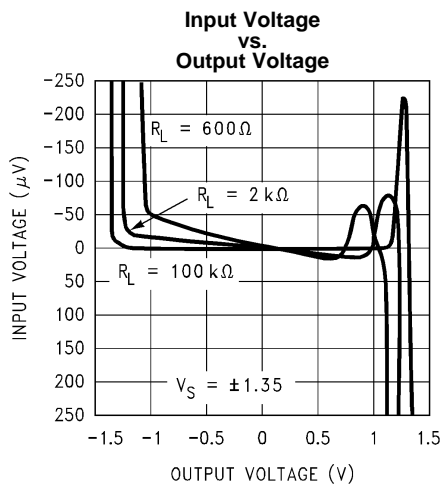


Figure 18.

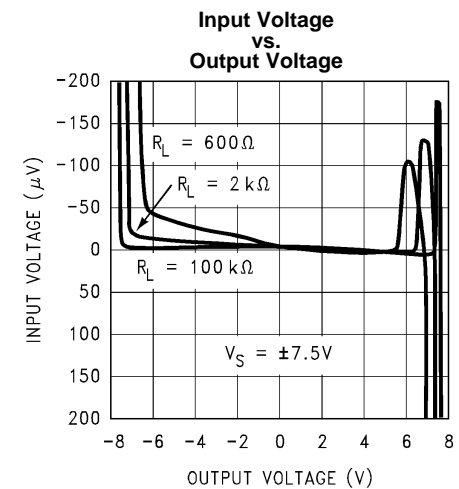


Figure 19.

## Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = 2.7V$ , single supply,  $T_A = 25^\circ C$

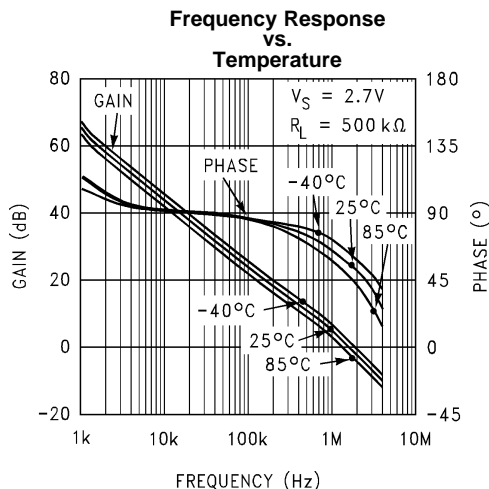


Figure 20.

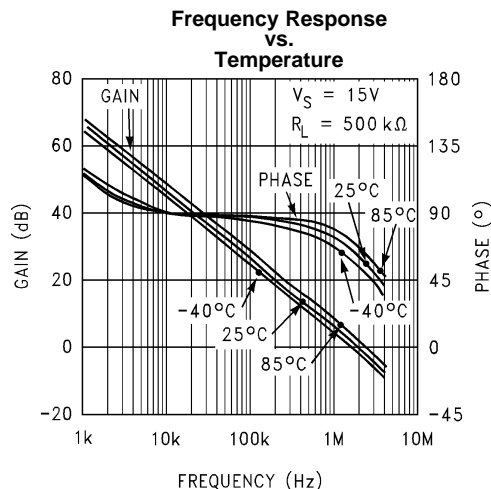


Figure 21.

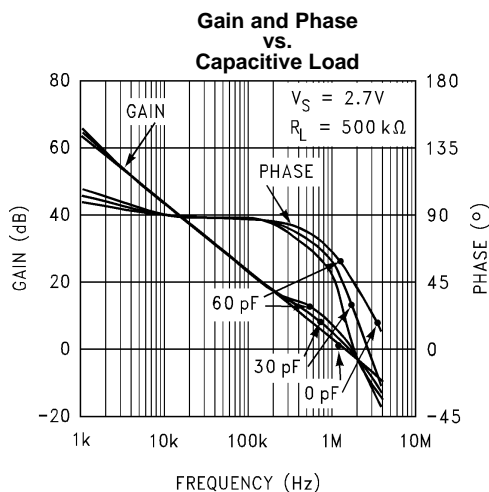


Figure 22.

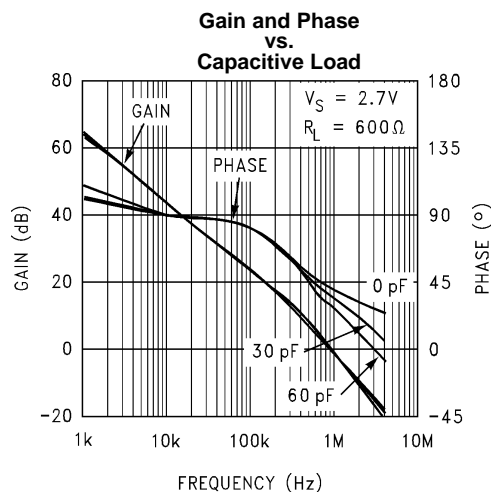


Figure 23.

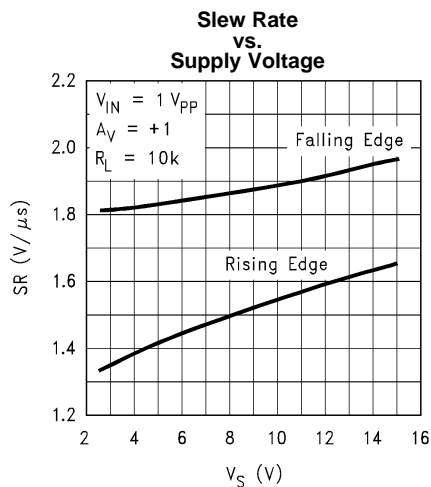


Figure 24.

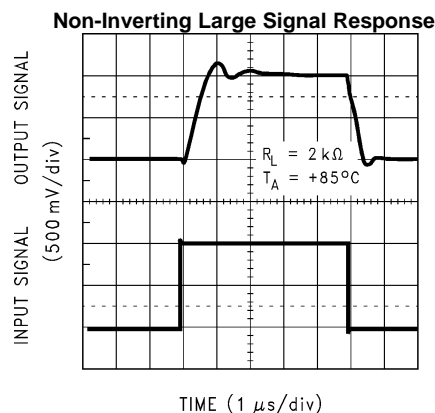
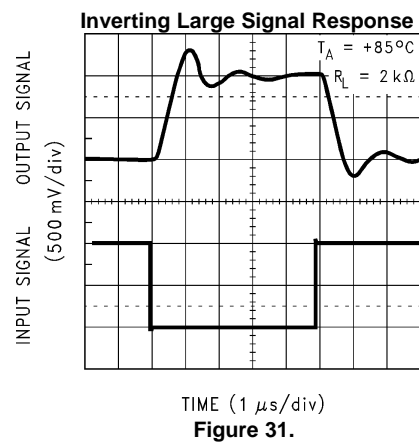
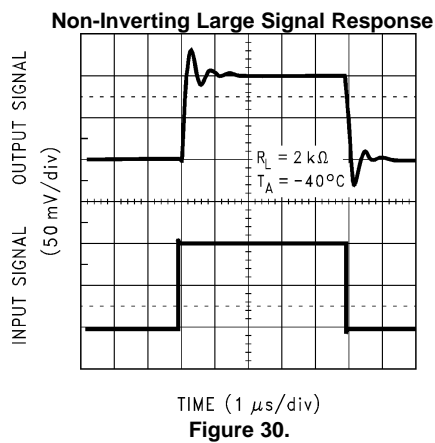
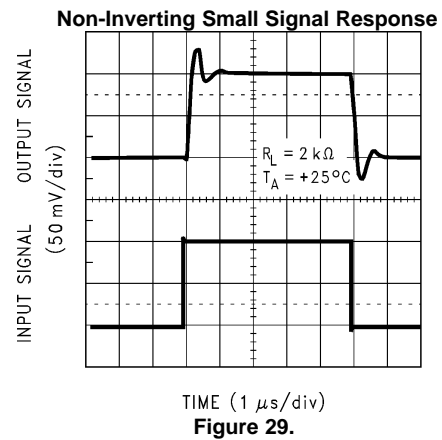
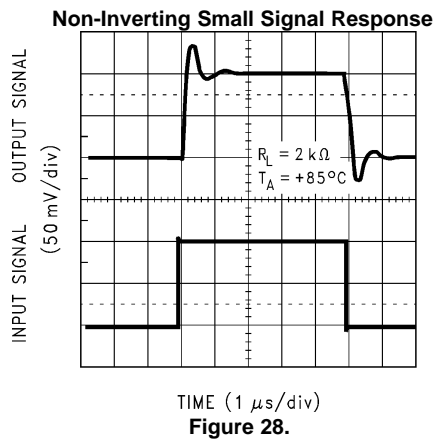
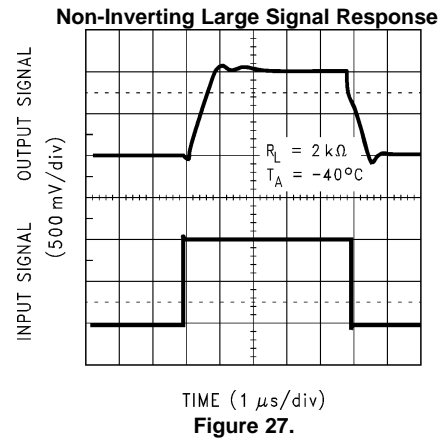
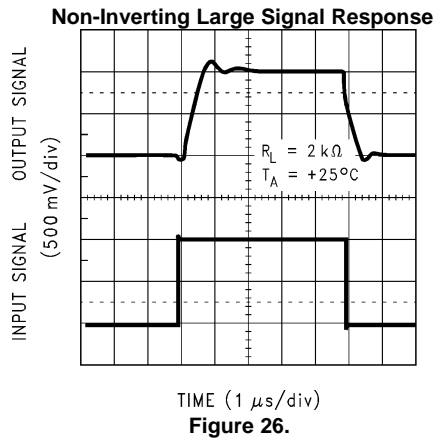


Figure 25.



## Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = 2.7V$ , single supply,  $T_A = 25^\circ C$



### Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = 2.7V$ , single supply,  $T_A = 25^\circ C$

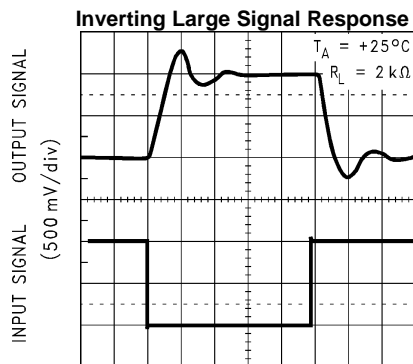
TIME (1  $\mu s$ /div)

Figure 32.

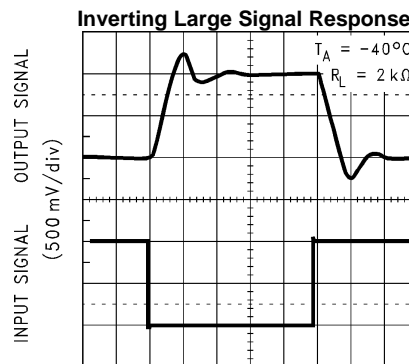
TIME (1  $\mu s$ /div)

Figure 33.

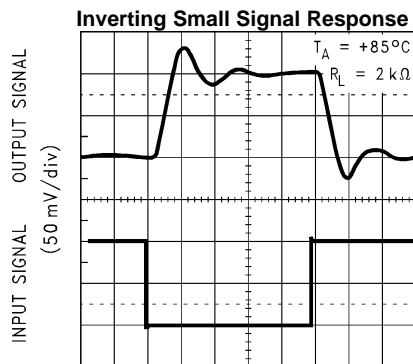
TIME (1  $\mu s$ /div)

Figure 34.

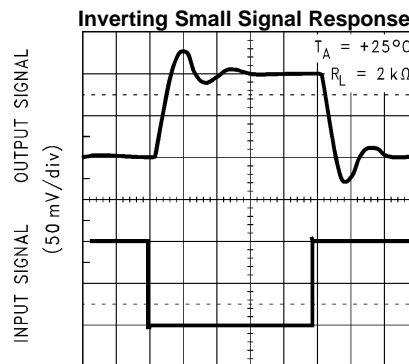
TIME (1  $\mu s$ /div)

Figure 35.

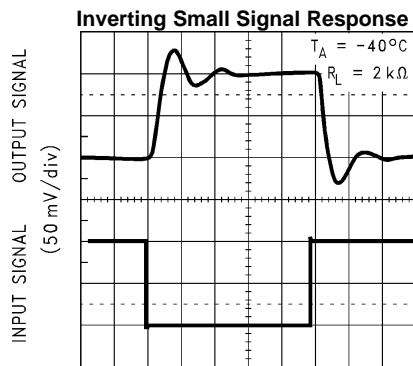
TIME (1  $\mu s$ /div)

Figure 36.

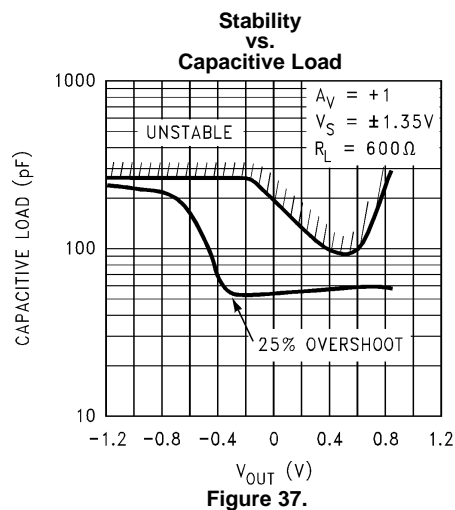
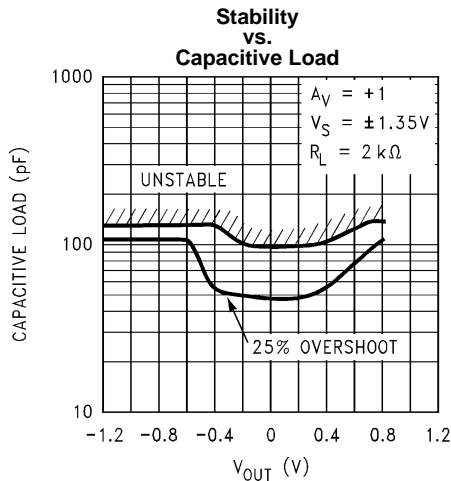


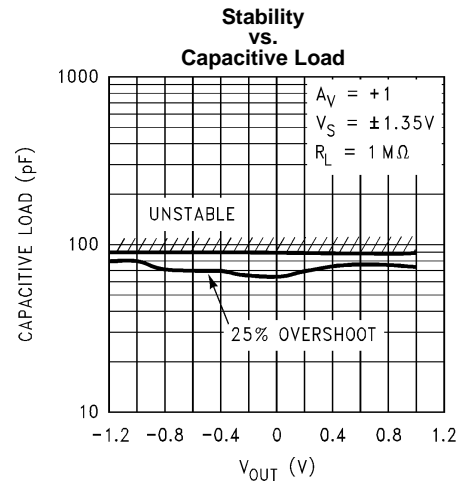
Figure 37.

## Typical Performance Characteristics (continued)

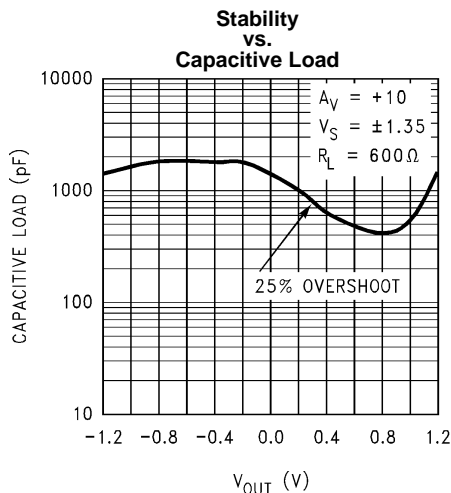
Unless otherwise specified,  $V_S = 2.7V$ , single supply,  $T_A = 25^\circ C$



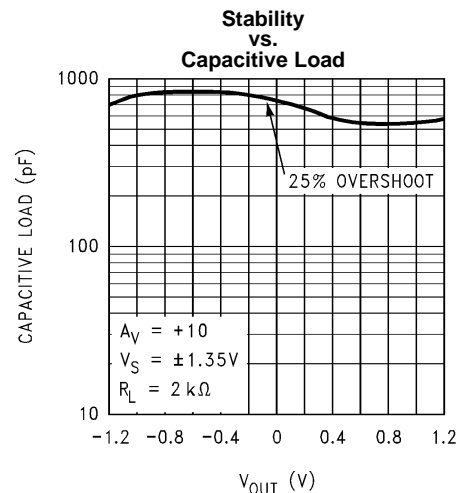
**Figure 38.**



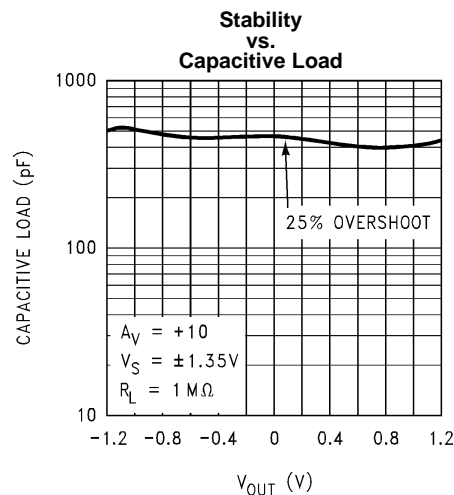
**Figure 39.**



**Figure 40.**



**Figure 41.**

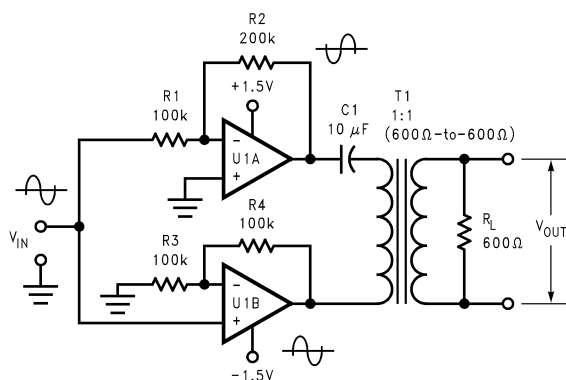


**Figure 42.**

## APPLICATION NOTES

### Background

The LMC6035/6 is exceptionally well suited for low voltage applications. A desirable feature that the LMC6035/6 brings to low voltage applications is its output drive capability—a hallmark for National's CMOS amplifiers. The circuit of [Figure 43](#) illustrates the drive capability of the LMC6035/6 at 3V of supply. It is a differential output driver for a one-to-one audio transformer, like those used for isolating ground from the telephone lines. The transformer (T1) loads the op amps with about 600Ω of AC load, at 1 kHz. Capacitor C1 functions to block DC from the low winding resistance of T1. Although the value of C1 is relatively high, its load reactance ( $X_c$ ) is negligible compared to inductive reactance ( $X_l$ ) of T1.



**Figure 43. Differential Driver**

The circuit in [Figure 43](#) consists of one input signal and two output signals. U1A amplifies the input with an inverting gain of  $-2$ , while the U1B amplifies the input with a non-inverting gain of  $+2$ . Since the two outputs are  $180^\circ$  out of phase with each other, the gain across the differential output is 4. As the differential output swings between the supply rails, one of the op amps sources the current to the load, while the other op amp sinks the current.

How good a CMOS op amp can sink or source a current is an important factor in determining its output swing capability. The output stage of the LMC6035/6—like many op amps—sources and sinks output current through two complementary transistors in series. This “totem pole” arrangement translates to a channel resistance ( $R_{dson}$ ) at each supply rail which acts to limit the output swing. Most CMOS op amps are able to swing the outputs very close to the rails—except, however, under the difficult conditions of low supply voltage and heavy load. The LMC6035/6 exhibits exceptional output swing capability under these conditions.

The scope photos of [Figure 44](#) and [Figure 45](#) represent measurements taken directly at the output (relative to GND) of U1A, in [Figure 43](#). [Figure 44](#) illustrates the output swing capability of the LMC6035, while [Figure 45](#) provides a benchmark comparison. (The benchmark op amp is another low voltage (3V) op amp manufactured by one of our reputable competitors.)

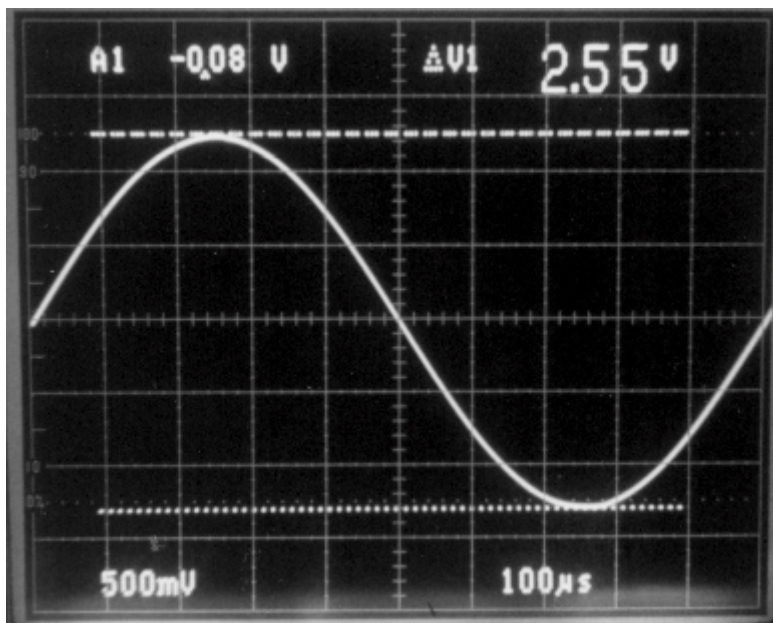


Figure 44. Output Swing Performance of the LMC6035 per the Circuit of [Figure 43](#)

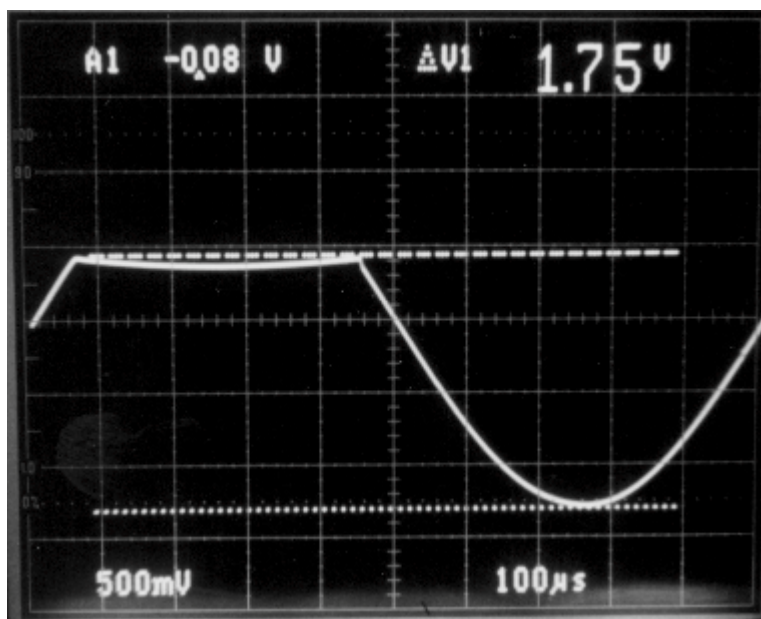


Figure 45. Output Swing Performance of Benchmark Op Amp per the Circuit of [Figure 43](#)

Notice the superior drive capability of LMC6035 when compared with the benchmark measurement—even though the benchmark op amp uses twice the supply current.

Not only does the LMC6035/6 provide excellent output swing capability at low supply voltages, it also maintains high open loop gain ( $A_{VOL}$ ) with heavy loads. To illustrate this, the LMC6035 and the benchmark op amp were compared for their distortion performance in the circuit of Figure 43. The graph of Figure 46 shows this comparison. The y-axis represents percent Total Harmonic Distortion (THD plus noise) across the loaded secondary of T1. The x-axis represents the input amplitude of a 1 kHz sine wave. (Note that T1 loses about 20% of the voltage to the voltage divider of  $R_L$  (600 $\Omega$ ) and T1's winding resistances—a performance deficiency of the transformer.)

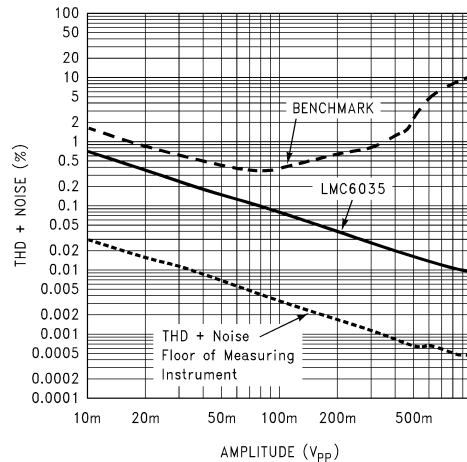


Figure 46. THD+Noise Performance of LMC6035 and “Benchmark” per Circuit of Figure 43

Figure 46 shows the superior distortion performance of LMC6035/6 over that of the benchmark op amp. The heavy loading of the circuit causes the  $A_{VOL}$  of the benchmark part to drop significantly which causes increased distortion.

## APPLICATION CIRCUITS

### Low-Pass Active Filter

A common application for low voltage systems would be active filters, in cordless and cellular phones for example. The ultra low input currents ( $I_{IN}$ ) of the LMC6035/6 makes it well suited for low power active filter applications, because it allows the use of higher resistor values and lower capacitor values. This reduces power consumption and space.

Figure 47 shows a low pass, active filter with a Butterworth (maximally flat) frequency response. Its topology is a Sallen and Key filter with unity gain. Note the normalized component values in parenthesis which are obtainable from standard filter design handbooks. These values provide a 1Hz cutoff frequency, but they can be easily scaled for a desired cutoff frequency ( $f_c$ ). The bold component values of Figure 47 provide a cutoff frequency of 3kHz. An example of the scaling procedure follows Figure 47.

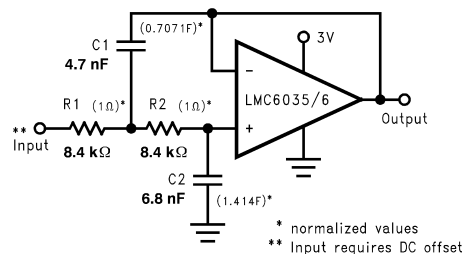


Figure 47. 2-Pole, 3kHz, Active, Sallen and Key, Lowpass Filter with Butterworth Response

## Low-Pass Frequency Scaling Procedure

The actual component values represented in bold of Figure 47 were obtained with the following scaling procedure:

1. First determine the frequency scaling factor (FSF) for the desired cutoff frequency. Choosing  $f_c$  at 3kHz, provides the following FSF computation:  

$$FSF = 2\pi \times 3\text{kHz} \text{ (desired cutoff freq.)} = 18.84 \times 10^3$$
2. Then divide all of the normalized capacitor values by the FSF as follows:  $C1' = C_{(\text{Normalized})}/FSF$   $C1' = 0.707/18.84 \times 10^3 = 37.93 \times 10^{-6}$   $C2' = 1.414/18.84 \times 10^3 = 75.05 \times 10^{-6}$  ( $C1'$  and  $C2'$ : prior to impedance scaling)
3. Last, choose an impedance scaling factor (Z). This Z factor can be calculated from a standard value for C2. Then Z can be used to determine the remaining component values as follows:

$$Z = C2'/C2_{(\text{chosen})} = 75.05 \times 10^{-6}/\mathbf{6.8nF} = 8.4k$$

$$C1 = C1'/Z = 37.93 \times 10^{-6}/8.4k = 4.52nF$$

$$\text{(Standard capacitor value chosen for C1 is } \mathbf{4.7nF} \text{ )} \quad R1 = R1_{(\text{normalized})} \times Z = 1\Omega \times 8.4k = 8.4k\Omega \quad R2 = R2_{(\text{normalized})} \times Z = 1\Omega \times 8.4k = 8.4k\Omega$$

(Standard value chosen for R1 and R2 is **8.45kΩ** )

## High Pass Active Filter

The previous low-pass filter circuit of Figure 47 converts to a high-pass active filter per Figure 48.

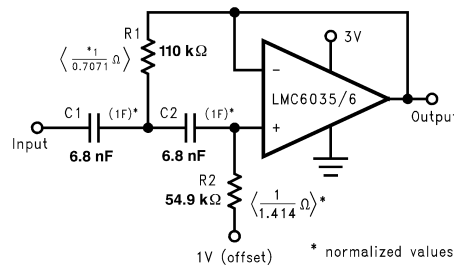


Figure 48. 2 Pole, 300Hz, Sallen and Key, High-Pass Filter

## High-Pass Frequency Scaling Procedure

Choose a standard capacitor value and scale the impedances in the circuit according to the desired cutoff frequency (300Hz) as follows:  $C = C1 = C2$   $Z = 1 \text{ Farad}/C_{(\text{chosen})} \times 2\pi \times (\text{desired cutoff freq.}) = 1 \text{ Farad}/\mathbf{6.8nF} \times 2\pi \times 300 \text{ Hz} = 78.05k$

$$R1 = Z \times R1_{(\text{normalized})} = 78.05k \times (1/0.707) = 110.4k\Omega$$

(Standard value chosen for R1 is **110kΩ** )

$$R2 = Z \times R2_{(\text{normalized})} = 78.05k \times (1/1.414) = 55.2k\Omega$$

(Standard value chosen for R1 is **54.9kΩ** )

## Dual Amplifier Bandpass Filter

The dual amplifier bandpass (DABP) filter features the ability to independently adjust  $f_c$  and Q. In most other bandpass topologies, the  $f_c$  and Q adjustments interact with each other. The DABP filter also offers both low sensitivity to component values and high Qs. The following application of Figure 49, provides a 1kHz center frequency and a Q of 100.

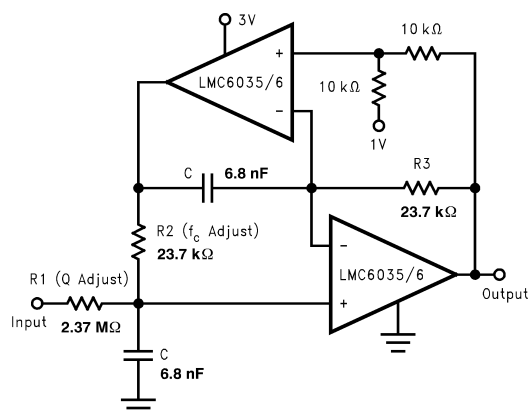


Figure 49. 2 Pole, 1kHz Active, Bandpass Filter

### DABP Component Selection Procedure

Component selection for the DABP filter is performed as follows:

1. First choose a center frequency ( $f_c$ ). Figure 49 represents component values that were obtained from the following computation for a center frequency of 1kHz.  $R2 = R3 = 1/(2\pi f_c C)$  Given:  $f_c = 1\text{kHz}$  and  $C$  (chosen) = **6.8nF**  $R2 = R3 = 1/(2\pi \times 1\text{kHz} \times 6.8\text{nF}) = 23.4\text{k}\Omega$   
 – (Chosen standard value is **23.7kΩ**)
2. Then compute R1 for a desired Q ( $f_c/\text{BW}$ ) as follows:  $R1 = Q \times R2$ . Choosing a Q of 100,  $R1 = 100 \times 23.7\text{k}\Omega = \mathbf{2.37M\Omega}$ .

### PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with  $< 1000\text{pA}$  of leakage current requires special layout of the PC board. If one wishes to take advantage of the ultra-low bias current of the LMC6035/6, typically  $< 0.04\text{pA}$ , it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may at times appear acceptably low. Under conditions of high humidity, dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6035 or LMC6036 inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See Figure 50. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of  $10^{12}\Omega$ , which is normally considered a very large resistance, could leak  $5\text{pA}$  if the trace were a  $5\text{V}$  bus adjacent to the pad of an input. This would cause a 100 times degradation from the amplifiers actual performance. However, if a guard ring is held within  $5\text{mV}$  of the inputs, then even a resistance of  $10^{11}\Omega$  would cause only  $0.05\text{pA}$  of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 51(a) through Figure 51(c) for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 51(d).



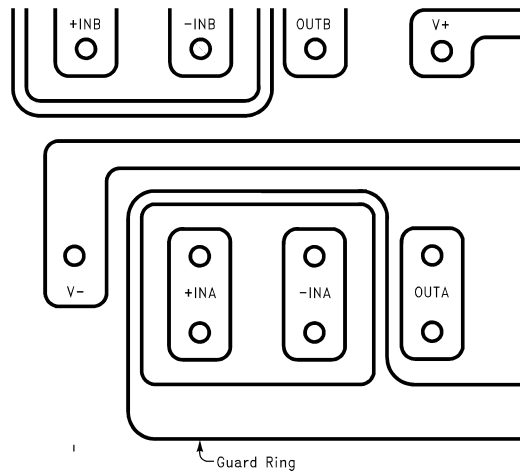


Figure 50. Example, using the LMC6036 of Guard Ring in PC Board Layout

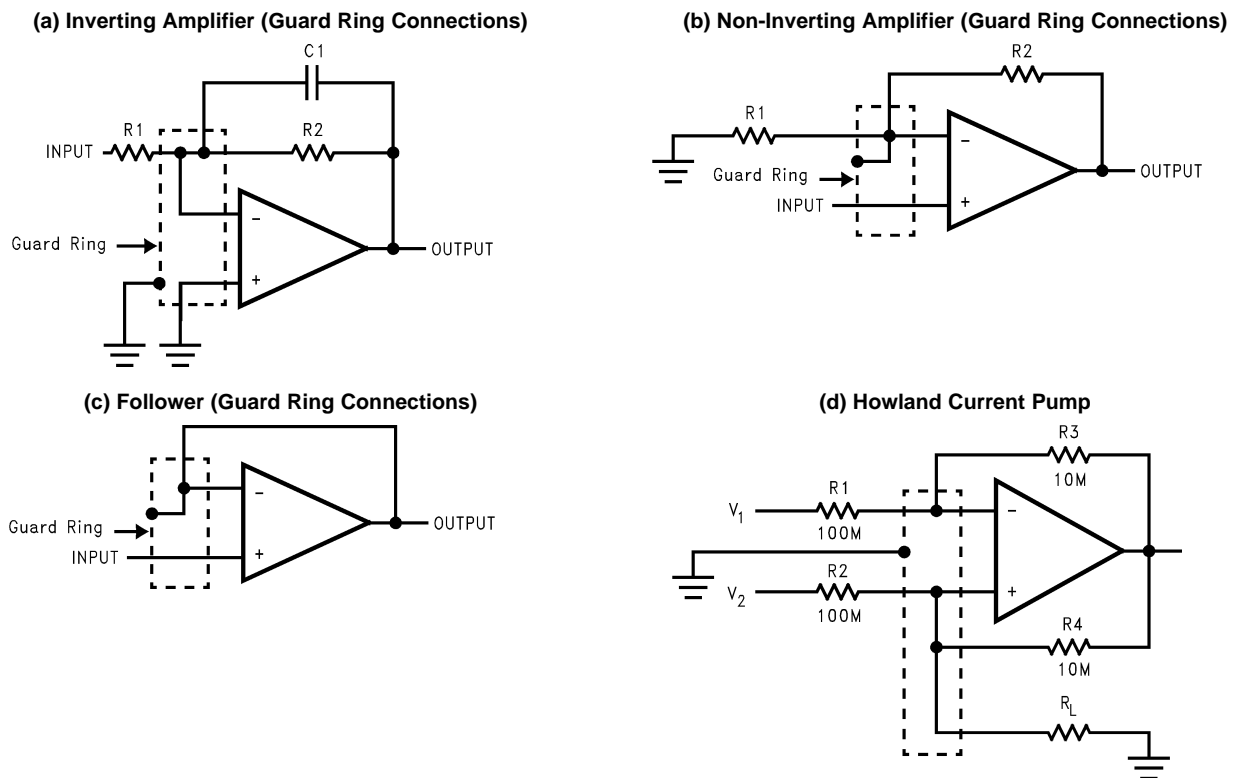


Figure 51. Guard Ring Connections

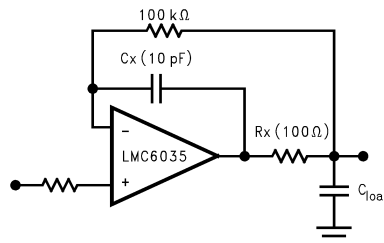
## CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6035/6 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in [Figure 52](#), the addition of a small resistor ( $50\Omega$ – $100\Omega$ ) in series with the op amp's output, and a capacitor ( $5\text{pF}$ – $10\text{pF}$ ) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

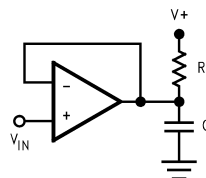
## DSBGA Considerations

Contrary to what might be guessed, the DSBGA package does not follow the trend of smaller packages having higher thermal resistance. LMC6035 in DSBGA has thermal resistance of  $220^\circ\text{C/W}$  compared to  $230^\circ\text{C/W}$  in VSSOP. Even when driving a  $600\Omega$  load and operating from  $\pm 7.5\text{V}$  supplies, the maximum temperature rise will be under  $4.5^\circ\text{C}$ . For application information specific to DSBGA, see Application note AN-1112.



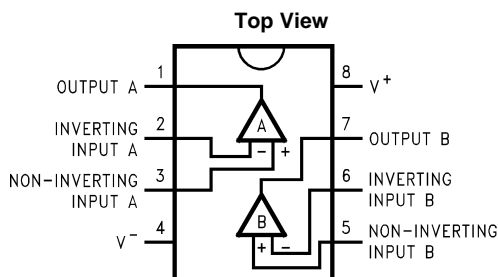
**Figure 52. Rx, Cx Improve Capacitive Load Tolerance**

Capacitive load driving capability is enhanced by using a pull up resistor to  $V^+$  ([Figure 53](#)). Typically a pull up resistor conducting  $500\mu\text{A}$  or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see [Electrical Characteristics](#)).

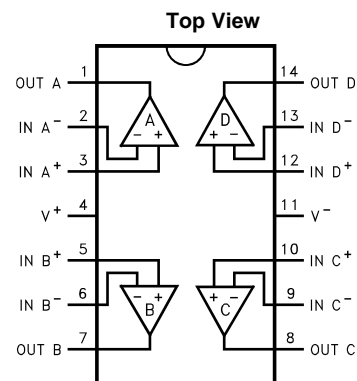


**Figure 53. Compensating for Large Capacitive Loads with a Pull Up Resistor**

## Connection Diagrams



**Figure 54. 8-Pin SOIC or VSSOP Package**  
See Package Number D0008A or DGK0008A



**Figure 55. 14-Pin SOIC or TSSOP Package**  
See Package Number D0014A or PW0014A

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMC6035IM	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMC6035IM	<a href="#">Samples</a>
LMC6035IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6035IM	<a href="#">Samples</a>
LMC6035IMM	ACTIVE	VSSOP	DGK	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A06B	<a href="#">Samples</a>
LMC6035IMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A06B	<a href="#">Samples</a>
LMC6035IMMX	ACTIVE	VSSOP	DGK	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	A06B	<a href="#">Samples</a>
LMC6035IMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A06B	<a href="#">Samples</a>
LMC6035IMX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMC6035IM	<a href="#">Samples</a>
LMC6035IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6035IM	<a href="#">Samples</a>
LMC6035ITL/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A80	<a href="#">Samples</a>
LMC6035ITLX/NOPB	ACTIVE	DSBGA	YZR	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	A80	<a href="#">Samples</a>
LMC6036IM	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMC6036IM	<a href="#">Samples</a>
LMC6036IM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6036IM	<a href="#">Samples</a>
LMC6036IMT	ACTIVE	TSSOP	PW	14	94	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	LMC6036IMT	<a href="#">Samples</a>
LMC6036IMT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6036IMT	<a href="#">Samples</a>
LMC6036IMTX	ACTIVE	TSSOP	PW	14	2500	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	LMC6036IMT	<a href="#">Samples</a>
LMC6036IMTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6036IMT	<a href="#">Samples</a>
LMC6036IMX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LMC6036IM	<a href="#">Samples</a>
LMC6036IMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6036IM	<a href="#">Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6035IMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6035IMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6035IMMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6035IMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6035IMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6035IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6035ITL/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LMC6035ITLX/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LMC6036IMTX	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMC6036IMTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMC6036IMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6036IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6035IMM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMC6035IMM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMC6035IMMX	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMC6035IMMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMC6035IMX	SOIC	D	8	2500	349.0	337.0	45.0
LMC6035IMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LMC6035ITL/NOPB	DSBGA	YZR	8	250	203.0	190.0	41.0
LMC6035ITLX/NOPB	DSBGA	YZR	8	3000	206.0	191.0	90.0
LMC6036IMTX	TSSOP	PW	14	2500	349.0	337.0	45.0
LMC6036IMTX/NOPB	TSSOP	PW	14	2500	349.0	337.0	45.0
LMC6036IMX	SOIC	D	14	2500	349.0	337.0	45.0
LMC6036IMX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0

## DGK (S-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

D (R-PDSO-G8)

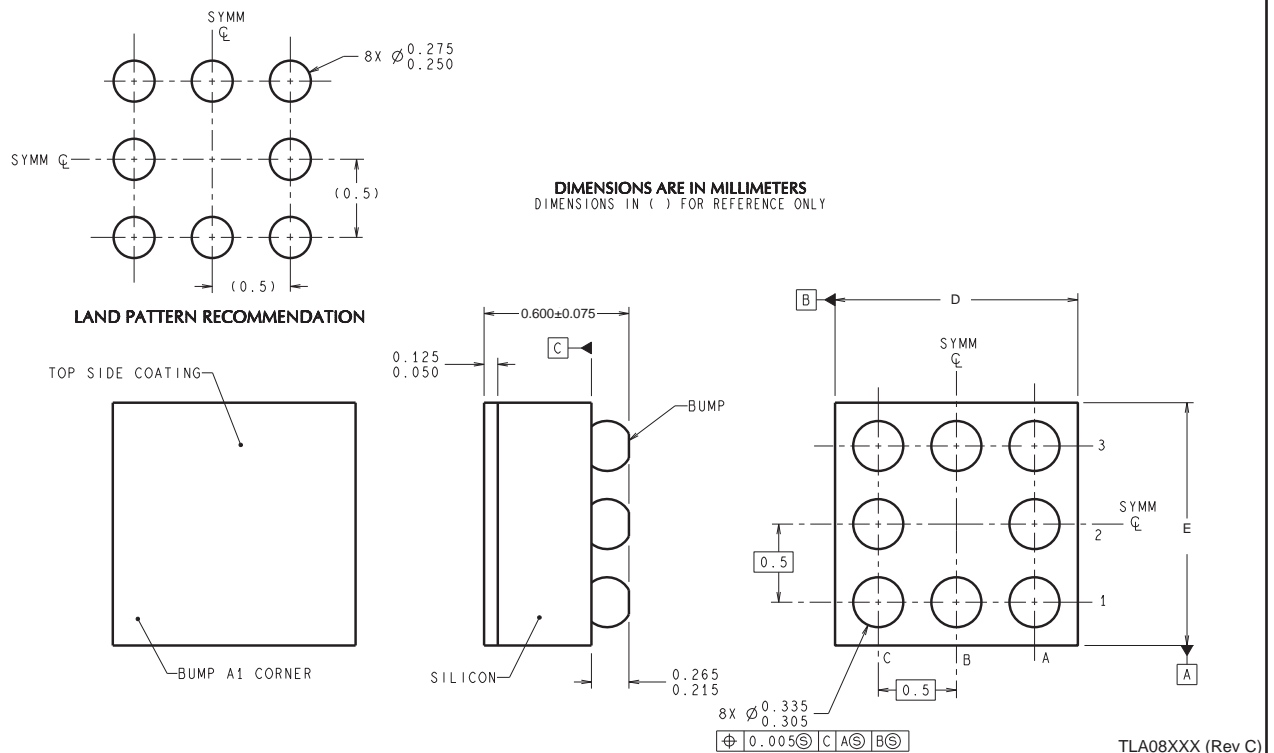
PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

YZR0008



D: Max = 1.941 mm, Min = 1.84 mm

E: Max = 1.788 mm, Min = 1.688 mm

4215045/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)