National Semiconductor

LMF120 Mask-Programmable Switched-Capacitor Active Filter System

General Description

The LMF120 is a mask-programmable switched-capacitor filter capable of realizing virtually any filter response up to twelve poles using six independent biquad blocks. It is customized to meet specific application requirements through the use of automated design techniques. Circuit realization occurs during the final metal-mask stage of the manufacturing process.

Three sample-and-hold inputs and three buffered outputs allow one, two, or three independent filters on a single chip. Each of the filters may be any type: high-pass, low-pass, all-pass, bandpass, or notch.

The center or cutoff frequency of each filter is determined by the clock frequency. The clock signal can be supplied by an external source, or it can be generated by the internal oscillator, using an external crystal and two capacitors. An on-board programmable divider chain can divide the clock input frequency by up to 256 so that each on-chip filter can have a different cutoff/center frequency. Accuracy is enhanced by close matching of the internal components: the ratio of the clock frequency to the center/corner frequency is typically accurate to ±0.5%, and is guaranteed to ±1.5% over the full temperature range.

The customization process is initiated by submitting transfer functions, pole and zero locations, or band diagrams to National Semiconductor. A worksheet is included in this datasheet, which can be returned to National Semiconductor for an initial evaluation. Each filter is computer-optimized to best meet the requested specifications, and computer simulations are produced for approval before prototyping begins.

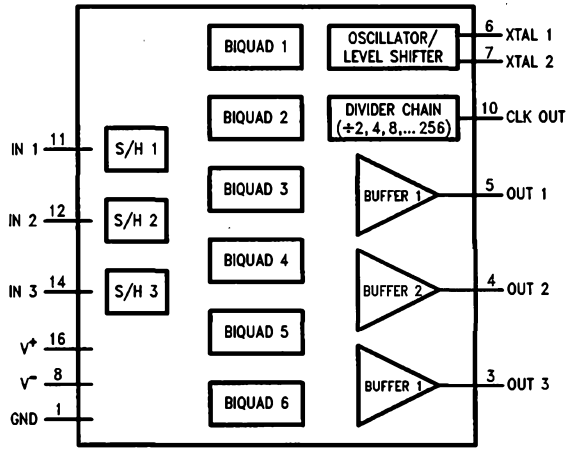
Features

- Mask-programmable for virtually any filter response
- All filter types (low-pass, high-pass, bandpass, notch, all-pass)
- All filter approximations (Butterworth, Chebyshev, Elliptic, Bessel, etc.)
- Up to 12 poles and right-half-plane zeros in one 16-pin package
- One, two, or three filters per package
- Wide Q range: up to 100 per biquad
- Choice of internal or external clock
- No external components other than clock or crystal and two capacitors
- Programmable clock divider: ÷2 to ÷256
- Center frequency accuracy: ±1.5% over temperature
- Supply voltage range: ±2V to ±7.5V or +4V to +14V

Applications

- Anti-alias filters
- Real-time audio analyzers
- Biomedical instrumentation
- Cellular telephones

Simplified Block Diagram



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Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage ($V^+ - V^-$)	−0.3V to +16V
Voltage at Any Pin	V^- − 0.3V to V^+ + 0.3V
Input Current per Pin (Note 10)	±5 mA
Total Input Current (Note 10)	±20 mA
Lead Temp. (Soldering 10 sec.)	
Dual-In-Line Package (Plastic)	300°C
Surface Mount Pkg. (Note 4)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Power Dissipation (Note 5)	500 mW
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility (Note 6)	2000V

Operating Ratings (Notes 2 & 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMF120CCN, LMF120CCV	$0°C \le T_A \le +70°C$
LMF120CIJ	$-40°C \le T_A \le +85°C$
LMF120CMJ	$-55°C \le T_A \le +125°C$
Supply Voltage ($V^+ - V^-$)	4.0V to 14V

Filter Electrical Characteristics

Because the LMF120's performance characteristics vary depending on the programming mask configuration, many of the specifications listed in this section are given only as typical values. These are intended to serve as guidelines for assessing the capabilities of the IC and the feasibility of a desired filter response. Specific filter performance data (obtained by computer simulation) will be supplied by National Semiconductor after the desired characteristics for the particular filter implementation have been defined. Test frequencies and attenuation values appropriate to the application can then be chosen. The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for T_{Min} to T_{Max}**; all other limits apply for $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Units (Limit)
f_{CLK}	Filter Clock Frequency		10 1.5			Hz (Min) MHz (Max)
f_{CLKIN}	Clock Input Frequency (Logic Circuitry Only)	Pin 6 or 7	4			MHz (Max)
f_0	Center or Cutoff Frequency		0.1 100			Hz (Min) kHz (Max)
f_{CLK}/f_0	Filter Clock-to-Center-Frequency Ratio Range (Each Biquad)		10 500			Hz/Hz (Min) Hz/Hz (Max)
$\Delta f_{CLK}/f_0$	Filter Clock-to-Center-Frequency Accuracy (Each Biquad)		±0.5			% (Max)
H_0	Passband Gain Error		±0.2			dB (Max)
Q	Filter "Q" (Each Biquad)		100			(Max)
$\frac{\Delta Q}{Q}$	Q Accuracy (Each Biquad)	$0.5 \le Q \le 30$	±2			%
$f_0 \times Q$	Center Frequency-Q Product	$Q \le 100$	1			MHz
	Dynamic Range (Each Biquad)	(Note 11)	80			dB
	Clock Feedthrough		10			mVrms
V_{OS}	Offset Voltage (Each Biquad)		70			mV
I_{SBQ}	Supply Current (Each Biquad)		0.4			mA
I_{SSH}	Supply Current (Each Input Sample-and-Hold)		0.3			mA
I_S	Total Supply Current (All Circuit Blocks Connected)		10			mA

Output Buffer Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for T_{Min} to T_{Max}**; all other limits apply for $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Units (Limit)
V_O	Output Voltage Swing	$R_L = 5\ k\Omega$		$V^+ - 1.0$ $V^- + 1.0$		V (Min) V (Max)
SR	Slew Rate		1.0			V/μs
C_L	Maximum Capacitive Load		200			pF
GBW	Gain-Bandwidth Product		1.0			MHz
I_S	Supply Current per Buffer		0.8			mA

Logic Input and Output Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for T_{Min} to T_{Max}**; all other limits apply for $T_A = T_J = +25°C$.

Symbol	Parameter		Conditions	Typical (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Units (Limit)
V_{IH} V_{IL}	Pin 7 CMOS Clock Input Voltage (Notes 12 and 13)	Logical "1" Logical "0"	$V^+ = 5V, V^- = -5V$		+3.0 −3.0		V (Min) V (Max)
V_{IH} V_{IL}		Logical "1" Logical "0"	$V^+ = 10V, V^- = 0V$		+8.0 +2.0		V (Min) V (Max)
V_{IH} V_{IL}		Logical "1" Logical "0"	$V^+ = 2.5V, V^- = -2.5V$		+1.5 −1.5		V (Min) V (Max)
V_{IH} V_{IL}		Logical "1" Logical "0"	$V^+ = 5V, V^- = 0V$		+4.0 +1.0		V (Min) V (Max)
V_{IH} V_{IL}	Pin 6 TTL Clock Input Voltage (Notes 12 and 13)	Logical "1" Logical "0"	$V^+ = 5V, V^- = -5V$		+2.0 +0.8		V (Min) V (Max)
V_{IH} V_{IL}		Logical "1" Logical "0"	$V^+ = 10V, V^- = 0V$		+2.0 +0.8		V (Min) V (Max)
V_{IH} V_{IL}		Logical "1" Logical "0"	$V^+ = 5V, V^- = 0V$		+2.0 +0.8		V (Min) V (Max)
V_{OH}	Clock Output	Logical "1"	$I_{OUT} = -1\ mA$		$V^+ - 1.0$		V (Min)
V_{OL}	Clock Output	Logical "0"	$I_{OUT} = +1\ mA$		$V^- + 1.0$		V (Max)
I_{IN}	Input Current	XTAL1, XTAL2			±10		μA (Max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is intended to be functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND unless otherwise specified.

Note 4: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any current Linear Data Book for other methods of soldering surface mount devices.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is a function of T_{Jmax}, Θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation, $T_{Jmax} = 125°C$. The typical thermal resistance (Θ_{JA}) of the LMF120N when board-mounted is 51°C/W. Θ_{JA} is typically 52°C/W for the LMF120J, and 86°C/W for the LMF120V.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typicals are at $T_J = 25°C$ and represent the most likely parametric norm.

Note 8: Tested Limits are guaranteed and 100% tested.

Note 9: Design Limits are guaranteed, but not 100% tested.

Note 10: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < V^-$ or $V_{IN} > V^+$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

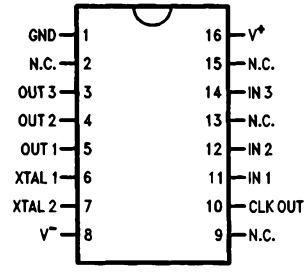
Note 11: Dynamic range is defined as the ratio of the tested minimum output voltage swing to the wideband noise over a 20 kHz bandwidth.

Note 12: Each custom version of the LMF120 will be tested at only one power supply voltage, which will be chosen to correspond to the application for which it is intended.

Note 13: Only one clock input will be active for any given version of the LMF120. Therefore, a device wil be tested for either TTL or CMOS clock input threshold, whichever is appropriate.

Connection Diagrams

Dual-In-Line Package



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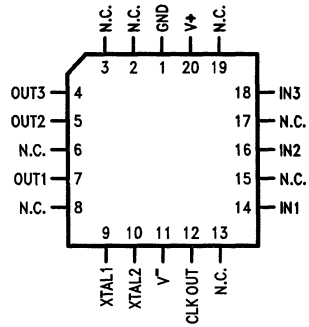
Order Number LMF120CIJ, LMF120CMJ, LMF120CCN
See NS Package Number J16A or N16E

Plastic Chip Carrier Package



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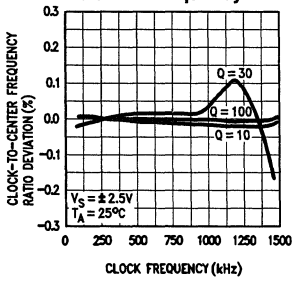
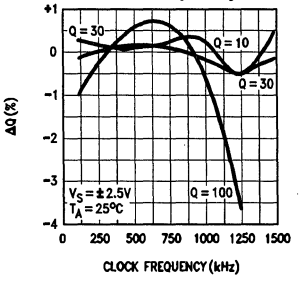
Order Number LMF120CCV
See NS Package Number V20A

Typical Performance Characteristics

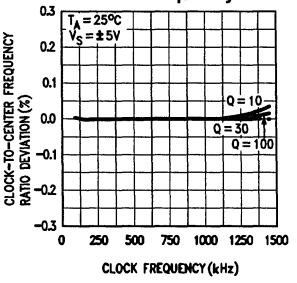
Biquad Clock-to-Center Frequency Ratio Deviation vs Clock Frequency



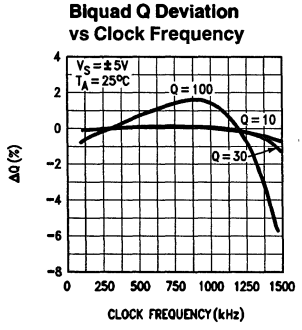
Biquad Q Deviation vs Clock Frequency



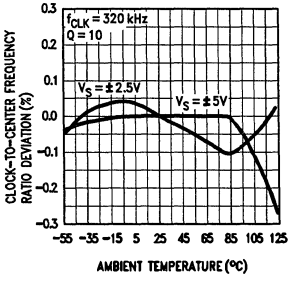
Biquad Clock-to-Center Frequency Ratio Deviation vs Clock Frequency



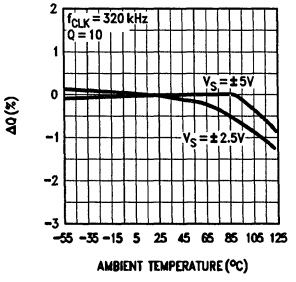
Biquad Q Deviation vs Clock Frequency



Biquad Clock-to-Center-Frequency Ratio Deviation vs Temperature



Biquad Q Deviation vs Temperature



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Pin Description

GND (Pin 1) This is the analog ground reference for the LMF120. In split supply applications, GND should be connected to the system ground. When operating the LMF120 from a single positive power supply voltage, pin 1 should be connected to a "clean" reference voltage midway between V^+ and V^-.

N.C. (Pins 2, 9, 13, & 15) These pins are not connected to the internal circuitry.

OUT3 (Pin 3), OUT2 (Pin 4), OUT1 (Pin 5) These are the outputs of the buffer amplifiers. Depending on the filter configuration, one, two, or all three of these outputs may be used.

XTAL1 (Pin 6) This is the crystal oscillator input pin. When using the internal oscillator, the crystal should be tied between XTAL1 and XTAL2. XTAL1 can also be used as an input for an external TTL-level clock.

XTAL2 Pin 7) This is the output of the internal crystal oscillator. When using the internal oscillator, the crystal should be tied between XTAL1 and XTAL2. XTAL2 can also be used as an input for an external CMOS logic-compatible clock swinging from V^+ to V^-.

V^- (Pin 8) This is the negative power supply pin. It should be bypassed with at least a 0.1 μF ceramic capacitor. For single-supply operation, connect this pin to system ground.

CLOCK OUT (Pin 10) This is the clock output pin. It can drive the clock inputs of additional filters or other components. The clock output signal swings from V^+ to V^-. This pin can be mask-programmed to supply an output at the same frequency as the internal oscillator or external clock input, or at any output frequency available from the internal divider chain.

INPUT1 (Pin 11), INPUT2 (Pin 12), INPUT3 (Pin 14) These are the inputs to the filter. When necessary (in notch filters, for example), the input pins are connected to the internal sample-hold circuits.

V^+ (Pin 16) This is the positive power supply pin. It should be bypassed with at least a 0.1 μF ceramic capacitor.

Functional Description

Each of the six internal biquad switched-capacitor filter sections (shown in detail in *Figure 1*) can have a characteristic equation of the form:

$$V_{OUT}(s) = \frac{S^2V_{HP} - V_{BP2}b_1s + V_{LP}b_0}{s^2 + a_1s + a_0} \quad (1)$$

or:

$$V_{OUT}(s) = \frac{-(s^2V_{HP} + V_{BP1}b_1s)}{s^2 + a_1s + a_0} \quad (2)$$

Note that by proper choice of coefficients and input connections, any type of filter response (low-pass, high-pass, bandpass, notch, or all-pass) can be obtained. For example, a notch filter can be realized by connecting the input signal to V_{HP} and V_{LP}. An all-pass filter can be realized by connecting the input signal to V_{HP}, V_{LP}, and V_{BP2}. Coefficients are controlled by the metal mask, which determines the values of the internal capacitors and the interconnections between the filter stages, sample-holds, and output buffers. By appropriate design of the metal mask, the biquad sections can be cascaded to form high-order filters.

The center or cutoff frequency is proportional to the filter clock frequency. The ratio of the clock frequency to the center frequency (f_{CLK}:f_0) is programmable with virtually infinite resolution over a range of 10:1 to 500:1, although clock-to-center-frequency ratios in the 50:1 to 100:1 range usually give the best performance.

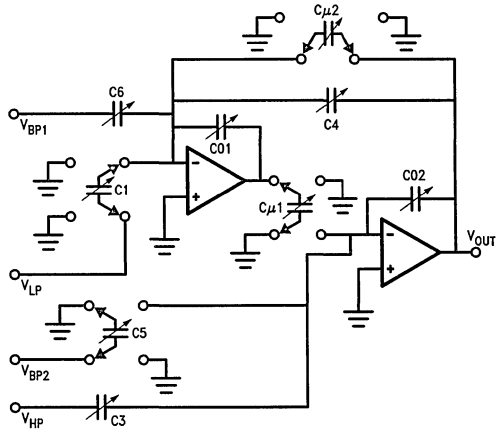

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FIGURE 1. Single Biquad Structure. There are six of these second-order blocks within the LMF120. Any of the biquad blocks can realize a low-pass, high-pass, bandpass, notch, or all-pass response.

The LMF120 contains three input sample-and-hold circuits. These are used only when necessary—in a notch filter, for example, where a sampled signal is summed with a continuous signal within the biquad. The result of such a summation would contain a residual signal equal to the difference between the sampled waveform and its continuous version. This residual would place a limit on the notch filter's effectiveness. The sample-and-hold ensures that the "continuous" signal path in the biquad (from V_{HP} to V_{OUT}) carries a sampled signal, thus improving the notch's performance.

In addition to three input pins, the LMF120 has three output buffer amplifiers, allowing one package to contain up to three independent filters. The total number of poles can be any number up to twelve, so, for example, a single LMF120 could perform the function of a 6th-order low-pass, a 2nd-order bandpass, and a 4th-order high-pass filter simultaneously.

Functional Description (Continued)

Clock Circuitry

The LMF120's clock input circuitry can be mask-programmed to accept an external TTL or CMOS-level clock, or to serve as a self-contained oscillator with the addition of an external crystal and two capacitors (see *Figure 6*). The clock signal can directly drive the biquad sections (if the frequency is appropriate), or its frequency can be divided by 2^n, where n is an integer between 1 and 8 ($\div 2$, $\div 4$, $\div 8$, ... $\div 256$). If necessary, each biquad section can obtain its clock signal from a different divider tap.

The Clock Output pin can be programmed to supply additional LMF120s or other circuits with a clock signal whose frequency is equal to either the clock input frequency, or the frequency at any of the divider taps.

Power Consumption

Because the LMF120 is a CMOS integrated circuit, its power consumption is low. To further reduce power consumption, any unused sample-and-holds and buffer amplifiers are shut down when fewer than three filters are required. (For example, a single 12th-order notch filter would need only one sample-and-hold and one buffer.) Unused biquad sections (if any) are shut down as well. For low-frequency applications, the internal current drain can be reduced by about 30% for further power savings.

Applications Information

Power Supplies

The LMF120 can operate from supply voltages ($V^+ - V^-$) ranging from 4.0V up to 14V, but the choice of supply voltage can affect circuit performance. The IC depends on MOS switches for its operation. All such switches have inherent "ON" resistances, which can cause small delays in charging internal capacitances. Increasing the supply voltage reduces this "ON" resistance, which improves the accuracy of the filter in high-frequency applications. The maximum practical center frequency improves by roughly 10% to 20% when the supply voltage increases from 5V to 10V.

Dynamic range is also affected by supply voltage. Both the noise level and the maximum signal voltage increase as supply voltage increases, but the maximum signal voltage increases more rapidly with supply voltage. Thus, the dynamic range is greater with higher supply voltages. It is therefore recommended that the supply voltage be kept near the maximum operating voltage when dynamic range and/or high-frequency performance are important.

As with all switched-capacitor filters, each of the LMF120's power supply pins should be bypassed with a minimum of 0.1 μF located close to the chip.

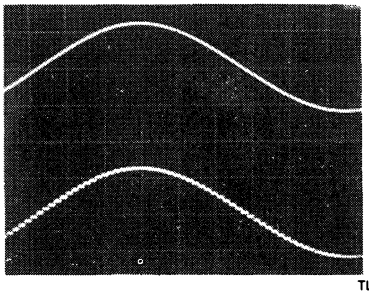

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FIGURE 2. Switched-Capacitor Filter Output Waveform. Note the sampling "steps".

SAMPLED-DATA SYSTEM CONSIDERATIONS

Output Steps

Because the LMF120 uses switched-capacitor techniques, its performance differs in several ways from non-sampled (continuous) circuits. The analog signal at any input is sampled during each filter clock cycle, and since the output voltage can change only once every clock cycle, the result is a discontinuous output signal. The output signal takes the form of a series of voltage "steps", as shown in *Figure 2*. The steps are smaller when the ratio of clock frequency to signal frequency is larger.

Aliasing

Another important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency, f_S. (The LMF120's sampling frequency is the same as the filter clock frequency). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled-data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_S/2 + 10$ Hz will cause the system to respond as though the input frequency was $f_S/2 - 10$ Hz. This phenomenon is known as "aliasing". Aliasing can be reduced or eliminated by limiting the input signal spectrum to less than $f_S/2$. In some cases, it may be necessary to use a bandwidth-limiting filter (often a simple passive RC low-pass) between the signal source and the switched-capacitor filter's input.

Clock Frequency Limitations

The performance characteristics of a switched-capacitor filter depend on the switching (clock) frequency. At very low clock frequencies (below 10 Hz), the time between clock cycles is relatively long, and small parasitic leakage currents cause the internal capacitors to discharge sufficiently to affect the filter's offset voltage and gain. This effect becomes more pronounced at elevated operating temperatures.

At higher clock frequencies, performance deviations are primarily due to the reduced time available for the internal operational amplifiers to settle. For this reason, when the filter clock is externally generated (clock divider unused), the clock waveform's duty cycle should be as close to 50% as possible, especially at high clock frequencies.

Offset Voltage

Switched-capacitor filters often have higher offset voltages than non-sampling filters with similar topologies. This is due to charge injection from the MOS switches into the sampling and integrating capacitors. The LMF120 is built using National's LMCMOS™ process for linear CMOS circuits, and has far lower input offset voltage than most other switched-capacitor filters. Typical offset voltage for an LMF120 filter will be in the 20 mV to 400 mV range, with the actual value being strongly dependent on the type of filter response being realized and the number of cascaded biquad stages needed to achieve that particular response.

Noise

Switched-capacitor filters have two kinds of noise at their outputs. There is a random, "thermal" noise component whose level is typically on the order of 250 μV. The actual value depends on the specific filter being implemented. The other kind of noise is digital clock feedthrough. This will have an amplitude in the vicinity of 10 mV rms. In some applications, the clock noise frequency is so high compared to the signal frequency that it is unimportant. In other cases,

Applications Information (Continued)

clock noise may have to be removed from the output signal with, for example, a passive low-pass filter at the LMF120's output.

Input Impedance

The LMF120's input pins may be connected to the sample-and-hold circuits or directly to biquad filter sections, depending on system requirements. The sample-and-hold input circuits, shown in the block diagram, are normally used only in filter implementations that require input signals (which are normally continuous) to be combined with sampled signals, as in notch and high-pass designs. Sampling the input before combining it with a sampled filter output makes the overall filter response more accurate.

During the first half of a clock cycle, the θ_1 switch closes, charging C_{IN} to the input voltage V_{IN}. During the second half-cycle, the θ_2 switch closes, and the charge on C_{IN} is transferred to the feedback capacitor. At frequencies well below the clock frequency, the input impedance approximates a resistor whose value is

$$R_{IN} = \frac{1}{C_{IN} f_{CLK}}.$$

At any sample/hold input, C_{IN} is nominally 0.5 pF. For a worst-case calculation of effective R_{IN}, assume C_{IN} = 0.5 pF and f_{CLK} = 1.5 MHz. Thus,

$$R_{in}(\text{min}) = \frac{1}{0.75 \times 10^{-6}} = 1.33\ \text{M}\Omega\ .$$

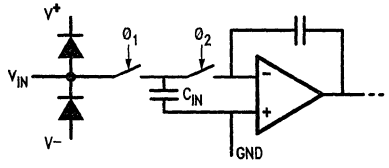

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FIGURE 3. The inputs to the sample-and-hold circuits consist of diodes, switches, and capacitors. The input impedance has a "resistive" component that depends on the clock frequency, and a capacitive component from the protection diodes.

At the maximum clock frequency of 1.5 MHz, the lowest typical value for the effective R_{IN} the V_{IN1} input is therefore 1.33 MΩ. Note that R_{IN} increases as f_{CLK} decreases, so the input impedance will always be greater than or equal to this value. In addition to this "resistive" input impedance, the input protection diodes and the package contribute a total of about 5 pF of capacitance from the input pin to ground.

When the input pins are connected directly to a biquad section, the input impedance can be either a "pure" capacitance to ground, or a "resistive" switched-capacitor network with characteristics similar to these of the sample-and-hold circuits. As *Figure 1* shows, the capacitors at the inputs of the biquads do not have fixed values. They are typically around 1 pF to 2 pF, but can be as large as 8 pF in some designs.

Typical Applications

Third-Octave Analyzer Filter

Figure 4 is a block diagram of one version of the LMF120. The LMF120-TPQ contains three fourth-order Chebyshev bandpass filters. The center frequencies are spaced ⅓ octave apart. This circuit is intended to be used in "real time" audio spectrum analysis applications. *Figure 5* shows the computer-simulated magnitude versus frequency curves for the LMF120-TPQ. These curves meet ANSI specifications for Type E, Class II, Third-Octave filters. The center frequencies of the LMF120-TPQ's three filters are located at $f_{CLK}/50$, $f_{CLK}/62.5$, and $f_{CLK}/80$, so that by using several LMF120-TPQs with clock frequencies separated by a factor

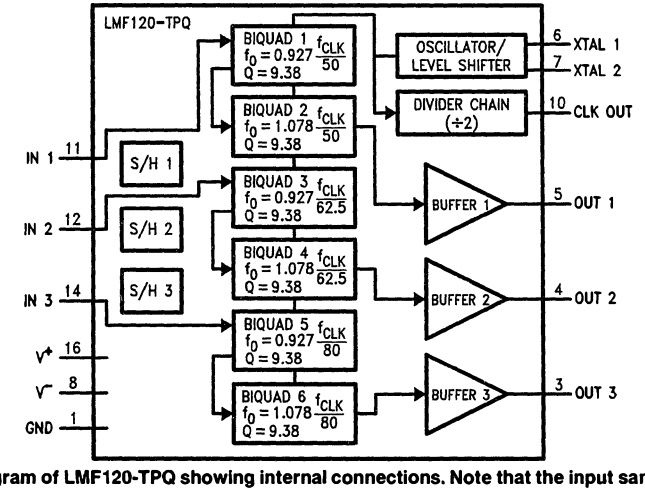

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FIGURE 4. Block Diagram of LMF120-TPQ showing internal connections. Note that the input sample-and-holds are not used in this version of the LMF120. The clock output frequency is one-half of the clock input frequency.

Typical Applications (Continued)

of 2n, a complex audio program can be analyzed for frequency content over a range of several octaves. To facilitate this, the CLK OUT pin of the LMF120-TPQ supplies an output clock signal whose frequency is ½ that of the incoming clock frequency. Therefore, a single internal or external clock oscillator can provide the clock reference for all of the 30 filters in a complete audio real time analyzer.

The circuit shown in *Figure 6* uses the LMF120-TPQ to implement a ⅓-octave filter set for use in "real time" audio program analyzers. Ten LMF120-TPQs can provide all of the filtering for the full audio frequency range.

The upper LMF120 handles the highest octave, with center frequencies of 20 kHz, 16 kHz, and 12.6 kHz. It also contains the 1 MHz master clock oscillator for the entire system. Its Clock Out pin provides a 500 kHz clock for the second LMF120, which supplies 250 kHz to the third LMF120, and so on.

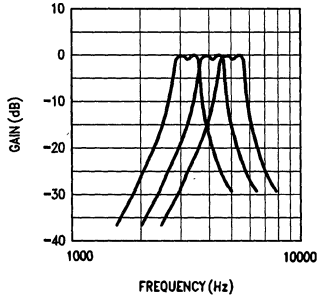

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FIGURE 5. Response curves for the three filters in the LMF120-TPQ. The clock frequency is 250 kHz.

If the audio input signal were applied to all of the LMF120-TPQ input pins, aliasing might occur in the lower frequency filters due to audio components near their clock frequencies (e.g., an input signal component near 1.8 kHz will produce an output from one of the filters in the LMF120 that handles the lowest octave). This problem is solved by using two LMF60-100 6th-order Butterworth low-pass filters as anti-aliasing filters. One LMF60-100 is placed ahead of the three lowest-frequency LMF120TPQs and is clocked with the 31.25 kHz clock signal. The other LMF60-100 is ahead of the next four LMF120-TPQs and the first LMF60-100. Its clock frequency is 500 kHz.

The internal sample-and-hold circuits are not connected to the LMF120-TPQ's input pins; instead, the inputs are connected directly to C6 of three of the biquads (see *Figure 4*). C6 is 1.2 pF in the LMF120-TPQ, so the input impedance at each input of the chip handling the highest octave will be 833 kΩ. The input impedances of the filters in the next octave will be twice this, or 1.667 MΩ, and so on. Each filter will also have 5 pF of additional capacitance to ground.

12th-Order Elliptic Low-Pass

With the internal biquads connected as shown in *Figure 7*, the LMF120 functions as a 12th-order elliptic low-pass filter with 0.4 dB passband ripple. The filter's extremely rapid cutoff slope is useful in applications such as anti-aliasing filters, where unwanted signals may exist at frequencies just above those of the desired signals. Two curves of gain vs frequency are included—*Figure 8* shows the filter's overall response, and *Figure 9* shows the passband response with much higher resolution.

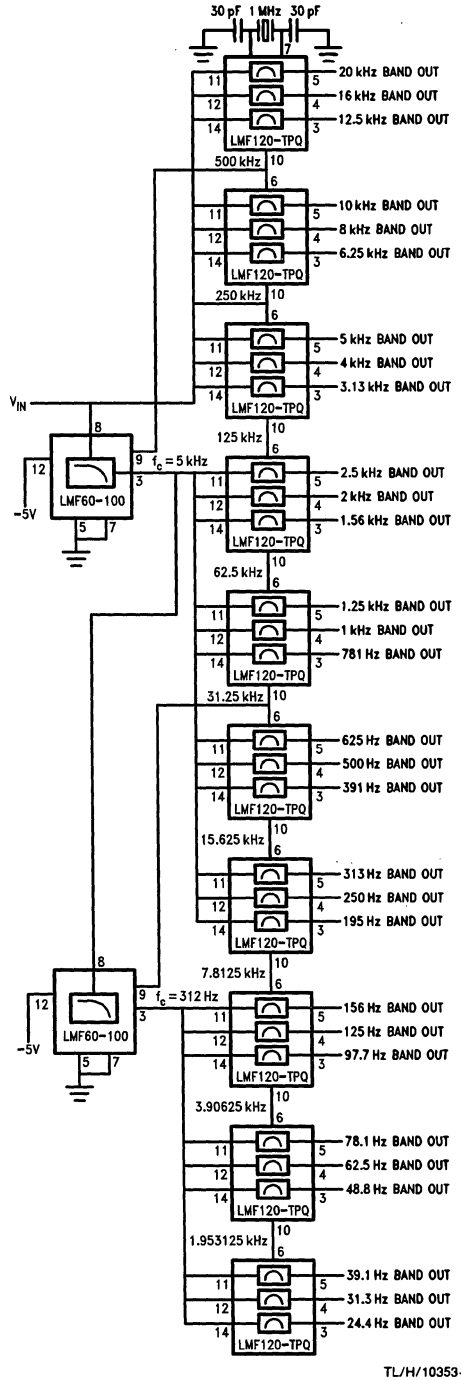

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FIGURE 6. Audio "Real-Time" analyzer filter set using LMF120-TPQ one-third octave filters. The LMF60s provide anti-alias filtering. Power supplies (not shown) are ±5V and should be bypassed with 0.1 μF at each supply pin.

Typical Applications (Continued)

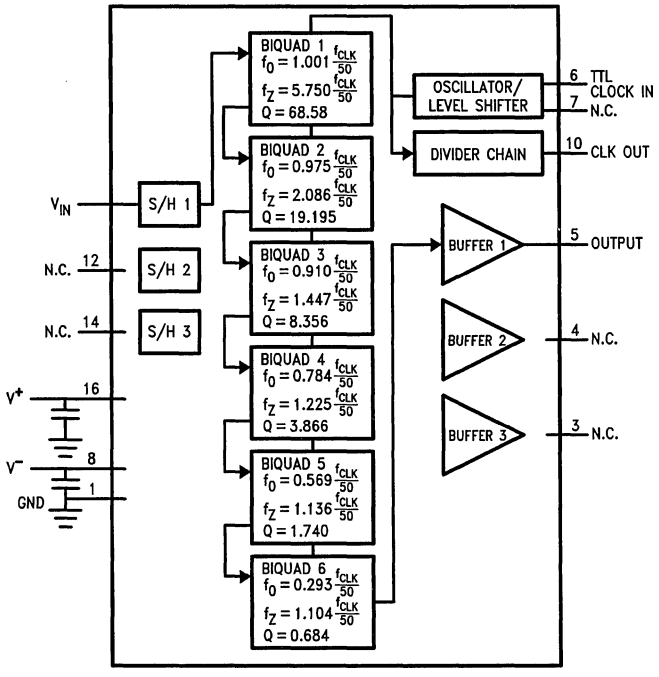

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FIGURE 7. 12th-Order Elliptic Low-Pass Filter

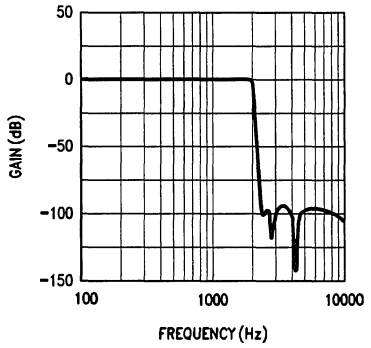

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FIGURE 8. Computer-simulated LMF120 12th-Order Elliptic Low-Pass Response. The clock frequency for the curve shown here is 100 kHz, and the clock-to-center-frequency ratio is 50:1.

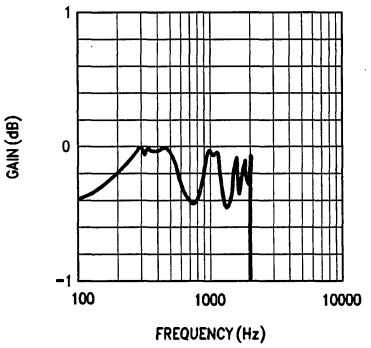

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FIGURE 9. Computer-simulated LMF120 12th-Order Elliptic Low-Pass Response. This curve covers the same frequency range as the one in *Figure 8*, but increased resolution shows the passband ripple more clearly.

Semi-Custom Filter Development Procedure

Note: Please contact the nearest National Semiconductor Sales Office for information on LMF120 semi-custom filter development costs.

Developing a new switched-capacitor filter using the LMF120 is relatively simple. First, define the performance requirements for the filter(s) in terms of pole and zero locations, transfer functions, or frequency/attenuation specifications, whichever is most convenient. The worksheet in the back of this data sheet may be used for this purpose. National Semiconductor will determine whether the application's performance requirements can be met with a semi-custom proprietary version of the LMF120. If the required filter is feasible, computer simulations of the filter's performance will be provided. If the performance is satisfactory, test frequencies and performance limits will be chosen and the custom metal mask will be produced and prototype devices will be manufactured. The prototyping stage generally takes from eight to twelve weeks. After prototypes have been built, tested, and approved, production can begin. (See the pre-production activity flow in *Figure 10*).

Feasibility

The first step in developing a custom filter based on the LMF120 is to determine whether an LMF120 can indeed realize the desired filter response. To this end, it is helpful to understand the limitations of the circuit.

The center or cutoff frequency (f_0) of the filter is one limitation. As indicated in the table of Filter Electrical Characteristics, this can typically range from a low of 0.1 Hz to a high of 100 kHz. These numbers, however, are given as guidelines only. The actual frequency limits will depend on the specific characteristics of the filter being developed. For example, if the desired filter must have a very fast attenuation slope beyond the cutoff frequency, the maximum cutoff frequency may be significantly less than 100 kHz. As a general rule, filters with gentler slopes can have cutoff frequencies as high as 100 kHz, while very fast rolloffs may be limited to corner frequencies below 20 kHz.

Filter Q is another parameter whose acceptable range is strongly dependent on the desired characteristics. Higher values of Q are more difficult to achieve with high center or corner frequencies. A useful figure of merit is the product of Q and F_0. If this product is less than 1 MHz and Q is less than 100 for each biquad filter section, it should be achievable with the LMF120.

Filter order is obviously an important specification. If the desired filter response requires a 13th-order filter, it can't be fully implemented by a single LMF120, which can provide up to 12 poles of filtering.

As discussed earier in this data sheet, the LMF120's offset voltage will generally be in the tens of millivolts, and will be dependent on the kind of transfer function the filter is intended to realize. It is important to ensure that the application's requirements are compatible with the LMF120's offset voltage characteristics.

THE DESIGN AUTOMATION SYSTEM

National Semiconductor customizes the LMF120 to a specific application by generating a metal mask that provides the interconnections between the internal circuit blocks and programs them for the required characteristics. The mask is generated using National's proprietary filter CAD software. This software computes the optimum capacitor values for each of the six switched-capacitor biquad filter sections to ensure close conformance to the target requirements. It also optimizes the design for high signal-to-noise ratio, and then analyzes the design, taking into account all second-order effects, such as parasitic capacitances, switch "ON" resistance, and the finite gain-bandwidth products of the operational amplifiers. The final design analysis is then returned for verification and approval.

Actual metal mask generation begins once the design and the test frequencies and limits have been approved. National's in-house CAD system is used to facilitate mask generation. The new metal mask is then used to complete the fabrication of the final silicon. The design automation system ensures fast and accurate results on the first run.

The Test Procedure

When the IC is in production, its performance must be verified by automated testing. Some of the tests will be common to all versions of the LMF120: logic levels and logic input current for example. Other tests will be for parameters that are specific to a particular metal mask. These consist of total supply current, DC offset voltages, signal swing, and several frequency/gain (or attenuation) test points for each filter. The frequencies and test limits will be tailored to the specific application requirements for the filter(s).

National will provide information on the typical behavior of the filter(s) for those parameters that are not tested or guaranteed by design, such as clock feedthrough and output noise. This information will be returned with the prototype parts.

Some special test requirements can be accommodated; these will be evaluated on request.

Semi-Custom Filter Development Procedure (Continued)

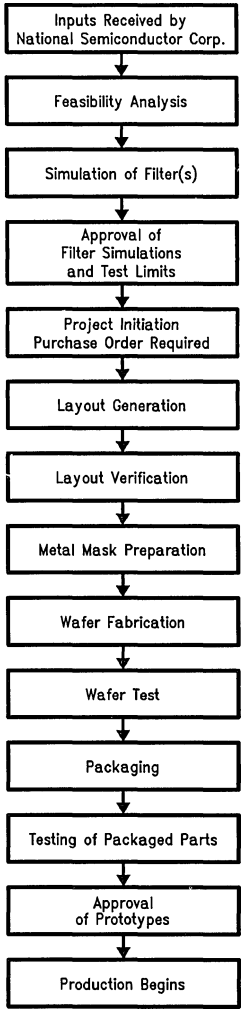

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FIGURE 10. Pre-Production Activity Flow

LMF120 Filter Worksheet Instructions

Use the following instructions for completing the attached Filter Worksheet. Return one completed worksheet for each LMF120 device (maximum of three filters per LMF120) to your local National Semiconductor sales office. If you require more worksheets you may photocopy this one.

1. Supply Voltage:

Specify your system supply voltage requirements. The total supply voltage ($V^+ - V^-$) can be anywhere from 4V to 14V. Higher voltages are advantageous when dynamic range and maximum operating frequency are critical concerns.

2. Total Number of Filters:

The LMF120 may consist of one, two or three independent filters. Specify the total number of filters for this LMF120 design.

3. Input Clock Frequency:

The maximum clock frequency is 4 MHz. Specify the crystal frequency if you plan to use the internal crystal oscillator. Two external capacitors and one crystal are required for the crystal oscillator.

4. Filter Clock Frequency:

This is the frequency at which the filter will be clocked. There are many factors to be considered in the choice of this frequency. Operation at the highest possible clock frequency reduces aliasing in the signal band, and reduces the need for pre- and/or post-filtering. However, there are certain factors that limit the maximum frequency. These include finite gain-bandwidth of the op-amps and finite on-resistances of internal switches. On the other hand, using slow clock frequencies enables the filter to operate at lower supply currents and to save power on applications requiring low-power operation. The maximum clock frequency for the LMF120's internal biquads is 1.5 MHz, so the internal clock frequency divider must be used to reduce this frequency if the clock frequency at the LMF120's clock input pin is greater than 1.5 MHz. Additionally, the filter clock frequency must also be at least ten times higher (and preferably 50 to 100 times higher) than the highest pole or zero in the filter structure.

Example: Determine the filter clock frequency for a BAND-PASS filter with center at 1 kHz. The system clock (input clock) is 3.5 MHz.

Solution: Since the input clock is higher than 1.5 MHz it must be divided down internally. Dividing by 32 gives a filter clock frequency of 109.38 kHz. Therefore, the clock-to-center frequency ratio is 109380/1000 = 109.38. This is close to the 50:1 to 100:1 range of clock-to-center-frequency ratios that generally gives the best results.

5. Clock Output Frequency:

This is an optional output that may be used to supply a clock frequency anywhere else in the application system. This output is subject to the following constraints:

$f_{CLKOUT} = f_{CLKIN}/2^n$ for n = 0, 1, . . . 8. Specify N/A if this output is not to be used.

6. Input Clock Level:

CMOS or TTL input levels may be specified for 0V–5V, ±5V or 0V–10V power supplies. For non-standard supplies, only CMOS input levels may be specified.

7. Filter Descriptions:

Use this space to describe the filter(s) by transfer functions, band diagrams, pole-zero locations, or f_0 and Q values for the individual biquads. Pole-zero locations or f_0 and Q values are preferred, but the filters may be described in any of the ways mentioned above. Examples of appropriate band diagrams are shown in *Figures 11* and *12*. f_C is the cutoff frequency of the passband and f_S is the frequency that defines the beginning of the stopband. A_{MAX} is the maximum acceptable passband gain variation. A_{MIN} is the minimum acceptable stopband attenuation.

LMF120 Filter Worksheet Instructions (Continued)

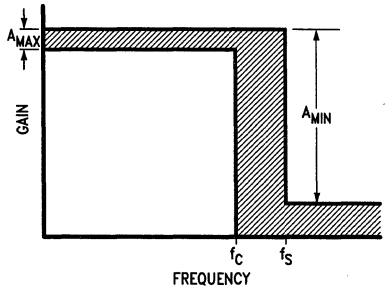

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FIGURE 11. Format of a band diagram for a low-pass filter. The amplitude response requirements are specified by A_{MAX}, A_{MIN}, f_C and f_S.

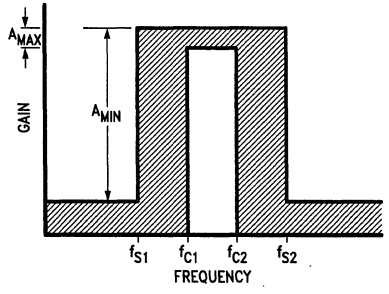

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FIGURE 12. Format of a band diagram for a bandpass filter. The filter's amplitude response requirements are specified by A_{MIN}, A_{MAX}, f_{C1}, f_{C2}, f_{S1} and f_{S2}.

Test frequencies for each filter should be specified with the following in mind:

A. Test frequencies between 100 Hz and 8 kHz: Digital Signal Processing techniques are used in the test procedure. This produces the best accuracy and allows the measurement of both amplitude and phase response at the test frequencies. The customer may choose between the following alternatives:

1. 7 test frequencies; each frequency is a multiple of 10 Hz with a minimum difference of 10 Hz.
2. 15 test frequencies; each frequency is a multiple of 10 Hz with a minimum difference of 20 Hz.

In the DSP test procedure, all of the test frequencies are applied to the filter simultaneously. The output energy available at any given frequency will be less with 15 test frequencies than with 7 test frequencies; therefore the test will be more accurate with 7 test frequencies than with 15 test frequencies.

B. Test frequencies above 8 kHz will require a voltmeter test method, which can measure only the amplitude response. The only constraint on the voltmeter method is that the test frequencies must be above 1 kHz. 7 frequencies can be tested.

Any special requirements will be considered separately, and may be included with the Worksheet.

8. APPLICATION INFORMATION:

Describe the application, the end product, and the most important performance characteristics for the filter in this application.

LMF120 Filter Worksheet

Engineering Contact _____

Phone _____

Company Name _____

Address _____

_____

_____

1) Supply Voltage _____

2) Total Number of Filters _____

3) Input Clock Frequency (4 MHz Maximum) _____

4) Filter Clock (1.5 MHz Maximum) _____

5) Clock Output Frequency _____

6) Input Clock Logic Levels (TTL or CMOS) _____

7) Filter Descriptions:

Please use the space below to define your filter(s). Note that the total sum of the poles or zeros for all three filters must not exceed twelve.

Filter #1

Filter Order _____

Use the space below to write the transfer function or pole/zero locations, or plot a detailed band diagram. Use a separate page if more space is needed.

Filter #1 Test Frequencies _____

_____

_____

_____

_____

_____

_____

Filter #2

Filter Order _____

Use the space below to write the transfer function or pole/zero locations, or plot a detailed band diagram. Use a separate page if more space is needed.

Filter #2 Test Frequencies _____

_____

_____

_____

_____

_____

_____

Filter #3

Filter Order _____

Use the space below to write the transfer function or pole/zero locations, or plot a detailed band diagram. Use a separate page if more space is needed.

Filter #3 Test Frequencies _____

_____

_____

_____

_____

_____

_____

8) Application Information: Please describe in detail the application for the LMF120 filters in your system.

a) End Product: _____

_____

b) Projected Volume per Year: _____

c) List the most important performance requirements for the filters in your application (i.e., Dynamic Range > 50 dB, etc.)