

# LMH6628 Dual Wideband, Low Noise, Voltage Feedback Op Amp

Check for Samples: LMH6628

### **FEATURES**

Wide unity gain bandwidth: 300MHz

Low noise: 2nV/√Hz

Low Distortion: -65/-74dBc (10MHz)

• Settling time: 12ns to 0.1%

• Wide supply voltage range: ±2.5V to ±6V

High output current: ±85mA

Improved replacement for CLC428

### **APPLICATIONS**

- High speed dual op amp
- · Low noise integrators
- · Low noise active filters
- Driver/receiver for transmission systems
- · High speed detectors
- I/Q channel amplifiers

### **DESCRIPTION**

The National LMH6628 is a high speed dual op amp that offers a traditional voltage feedback topology featuring unity gain stability and slew enhanced circuitry. The LMH6628's low noise and very low harmonic distortion combine to form a wide dynamic range op amp that operates from a single (5V to 12V) or dual (±5V) power supply.

Each of the LMH6628's closely matched channels provides a 300MHz unity gain bandwidth and low input voltage noise density (2nV/\/Hz). Low 2nd/3rd harmonic distortion (-65/-74dBc at 10MHz) make the LMH6628 a perfect wide dynamic range amplifier for matched I/Q channels.

With its fast and accurate settling (12ns to 0.1%), the LMH6628 is also an excellent choice for wide dynamic range, anti-aliasing filters to buffer the inputs of hi resolution analog-to-digital converters. Combining the LMH6628's two tightly matched amplifiers in a single 8-pin SOIC package reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

The LMH6628 is fabricated using National's VIP10™ complimentary bipolar process.

To reduce design times and assist in board layout, the LMH6628 is supported by an evaluation board (CLC730036).

#### **Connection Diagram**

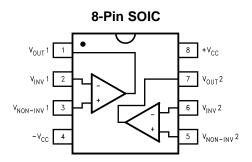


Figure 1. Top View

A

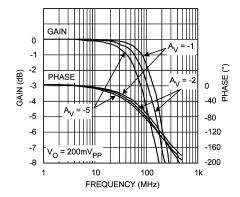
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## **Inverting Frequency Response**





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Human Body Model	2kV
Machine Model	200V
Supply Voltage	13.5
Short Circuit Current	(3)
Common-Mode Input Voltage	V+ - V <sup>-</sup>
Differential Input Voltage	V+ - V <sup>-</sup>
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering 10 sec)	+300°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.
- (2) Human body model,  $1.5k\Omega$  in series with 100pF. Machine model,  $0\Omega$  In series with 200pF.
- (3) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

# Operating Ratings (1)

operating matinge		
Thermal Resistance (2)		
Package	$(\theta_{\sf JC})$	$(\theta_{JA})$
SOIC	65°C/W	145°C/W
Temperature Range		−40°C to +85°C
Nominal Supply Voltage		±2.5V to ±6V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.
- (2) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$  and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)}^- T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC board.



# Electrical Characteristics (1)

 $V_{CC}$  = ±5V,  $A_V$  = +2V/V,  $R_F$  = 100 $\Omega$ ,  $R_G$  = 100 $\Omega$ ,  $R_L$  = 100 $\Omega$ ; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
Frequency	Domain Response			•		1
GB	Gain Bandwidth Product	$V_O < 0.5V_{PP}$		200		MHz
SSBW	-3dB Bandwidth, A <sub>V</sub> = +1	V <sub>O</sub> < 0.5V <sub>PP</sub>	180	300		MHz
SSBW	-3dB Bandwidth, A <sub>V</sub> = +2	$V_O < 0.5V_{PP}$		100		MHz
GFL	Gain Flatness	V <sub>O</sub> < 0.5V <sub>PP</sub>				
GFP	Peaking	DC to 200MHz		0.0		dB
GFR	Rolloff	DC to 20MHz		.1		dB
LPD	Linear Phase Deviation	DC to 20MHz		.1		deg
Time Doma	ain Response					
TR	Rise and Fall Time	1V Step		4		ns
TS	Settling Time	2V Step to 0.1%		12		ns
OS	Overshoot	1V Step		1		%
SR	Slew Rate	4V Step	300	550		V/µs
Distortion	And Noise Response	-				
HD2	2nd Harmonic Distortion	1V <sub>PP</sub> , 10MHz		-65		dBc
HD3	3rd Harmonic Distortion	1V <sub>PP</sub> , 10MHz		-74		dBc
	Equivalent Input Noise					
$V_N$	Voltage	1MHz to 100MHz		2		nV/√Hz
I <sub>N</sub>	Current	1MHz to 100MHz		2		pA/√Hz
XTLKA	Crosstalk	Input Referred, 10MHz		-62		dB
Static, DC	Performance					
G <sub>OL</sub>	Open-Loop Gain		56 <b>53</b>	63		dB
V <sub>IO</sub>	Input Offset Voltage			±.5	±2 <b>±2.6</b>	mV
DV <sub>IO</sub>	Average Drift			5		μV/°C
I <sub>BN</sub>	Input Bias Current			±.7	±20 ± <b>30</b>	μA
DI <sub>BN</sub>	Average Drift			150		nA/°C
Ios	Input Offset Current			0.3	±6	μΑ
I <sub>OSD</sub>	Average Drift			5		nA/°C
PSRR	Power Supply Rejection Ratio		60 <b>46</b>	70		dB
CMRR	Common-Mode Rejection Ratio		57 <b>54</b>	62		dB
I <sub>CC</sub>	Supply Current	Per Channel, R <sub>L</sub> = ∞	7.5 <b>7.0</b>	9	12 <b>12.5</b>	mA
Miscellane	ous Performance	·	-	+		+
R <sub>IN</sub>	Input Resistance	Common-Mode		500		kΩ
		Differential-Mode		200		kΩ
C <sub>IN</sub>	Input Capacitance	Common-Mode		1.5		pF
		Differential-Mode		1.5		pF
R <sub>OUT</sub>	Output Resistance	Closed-Loop		.1		Ω

<sup>(1)</sup> Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where T<sub>J</sub> > T<sub>A</sub>. See Note 6 for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.



# **Electrical Characteristics** (1) (continued)

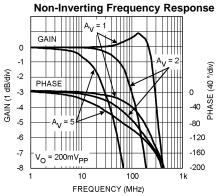
 $V_{CC}$  = ±5V,  $A_V$  = +2V/V,  $R_F$  = 100 $\Omega$ ,  $R_G$  = 100 $\Omega$ ,  $R_L$  = 100 $\Omega$ ; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
Vo	Output Voltage Range	R <sub>L</sub> = ∞		±3.8		٧
V <sub>OL</sub>		$R_L = 100\Omega$	±3.2 ±3.1	±3.5		V
CMIR	Input Voltage Range	Common- Mode		±3.7		V
Io	Output Current		±50	±85		mA

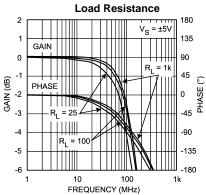


## **Typical Performance Characteristics**

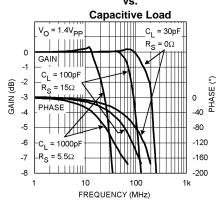
 $(T_A = +25^\circ, A_V = +2, V_{CC} = \pm 5V, R_f = 100\Omega, R_L = 100\Omega, unless specified)$ 

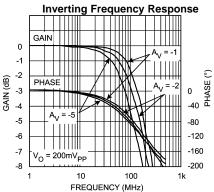


# Frequency Response

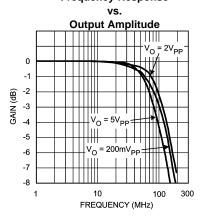


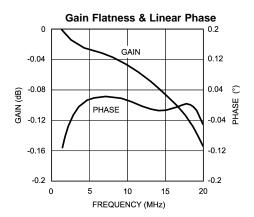
# Frequency Response





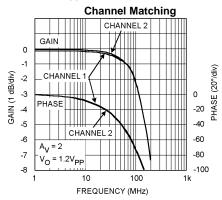
## Frequency Response

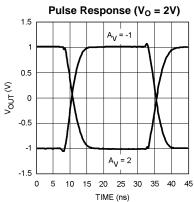


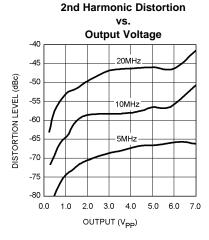


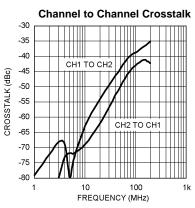


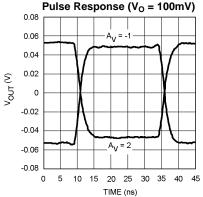
 $(T_A = +25^\circ, A_V = +2, V_{CC} = \pm 5V, R_f = 100\Omega, R_L = 100\Omega, unless specified)$ 











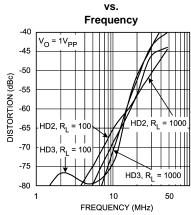
**3rd Harmonic Distortion** 

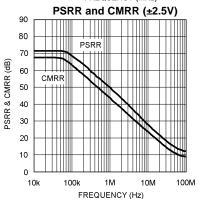
vs. **Output Voltage** -20 -30 20MHz DISTORTION LEVEL (dBc) -40 -50 10MHz -60 5MHz -80 0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.C OUTPUT (V<sub>PP</sub>)

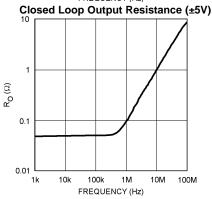


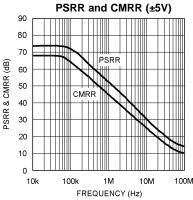
 $(T_A = +25^\circ, A_V = +2, V_{CC} = \pm 5V, R_f = 100\Omega, R_L = 100\Omega, unless specified)$ 

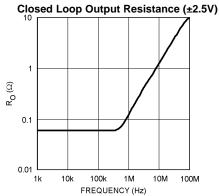
## 2nd & 3rd Harmonic Distortion

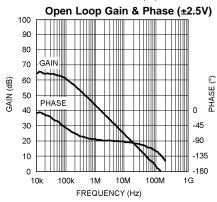






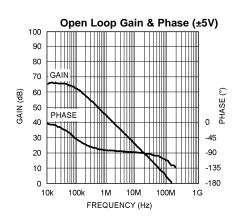


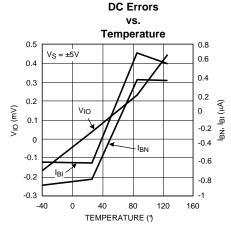


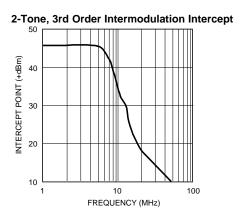


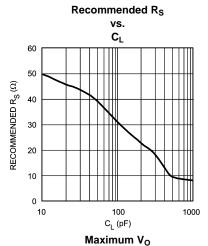


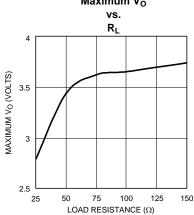
 $(T_A$  = +25°,  $A_V$  = +2,  $V_{CC}$  = ±5V,  $R_f$  =100 $\Omega$ ,  $R_L$  = 100 $\Omega$ , unless specified)











VS.
Frequency

1000

CURRENT NOISE

1000

VOLTAGE NOISE

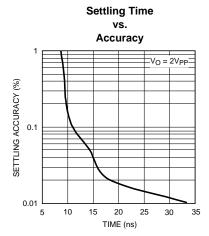
1 10 100 1k 10k 100k 1M 10M

FREQUENCY (Hz)

**Voltage & Current Noise** 



 $(T_A = +25^\circ, A_V = +2, V_{CC} = \pm 5V, R_f = 100\Omega, R_L = 100\Omega, unless specified)$ 



## **Application Section**

### **LOW NOISE DESIGN**

Ultimate low noise performance from circuit designs using the LMH6628 requires the proper selection of external resistors. By selecting appropriate low valued resistors for  $R_F$  and  $R_G$ , amplifier circuits using the LMH6628 can achieve output noise that is approximately the equivalent voltage input noise of  $2nV/\sqrt{\text{Hz}}$  multiplied by the desired gain  $(A_V)$ .

#### DC BIAS CURRENTS AND OFFSET VOLTAGES

Cancellation of the output offset voltage due to input bias currents is possible with the LMH6628. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage ( $V_{OS}$ ) multiplied by the desired gain ( $A_V$ ). National Application Note OA-7 offers several solutions to further reduce the output offset.

### **OUTPUT AND SUPPLY CONSIDERATIONS**

With  $\pm 5$ V supplies, the LMH6628 is capable of a typical output swing of  $\pm 3.8$ V under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than  $50\Omega$ , the output swing will be limited by the LMH6628's output current capability, typically 85mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See the plot labeled " $R_S$  vs.  $C_L$ " in the Typical Performance section.

#### **LAYOUT**

Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of 0.1µF should be placed as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 for more information. National suggests the 730036 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

#### **ANALOG DELAY CIRCUIT (ALL-PASS NETWORK)**

The circuit in Figure 2 implements an all-pass network using the LMH6628. A wide bandwidth buffer (LM7121) drives the circuit and provides a high input impedance for the source. As shown in Figure 3, the circuit provides a 13.1ns delay (with R =  $40.2\Omega$ , C = 47pF).  $R_F$  and  $R_G$  should be of equal and low value for parasitic insensitive operation.



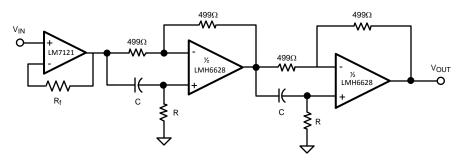


Figure 2. Circuit That Implements an All-pass Network Using the LMH6628

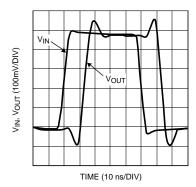


Figure 3. Delay Circuit Response to 0.5V Pulse

The circuit gain is +1 and the delay is determined by the following equations.

$$^{\tau} delay = 2(2RC + T_d)$$
 (1)

$$T_{d} = \frac{1}{360} \frac{d\phi}{df};$$

where  $T_d$  is the delay of the op amp at  $A_V = +1$ .

The LMH6628 provides a typical delay of 2.8ns at its -3dB point.

### **FULL DUPLEX DIGITAL OR ANALOG TRANSMISSION**

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The LMH6628's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in Figure 4, one of the LMH6628's amps is used as a "driver" and the other as a difference "receiver" amplifier. The output impedance of the "driver" is essentially zero. The two R's are chosen to match the characteristic impedance of the transmission line. The "driver" op amp gain can be selected for unity or greater.

Receiver amplifier  $A_2$  ( $B_2$ ) is connected across R and forms differential amplifier for the signals transmitted by driver  $A_2$  ( $B_2$ ). If  $R_F$  equals  $R_G$ , receiver  $A_2$  ( $B_1$ ) will then reject the signals from driver  $A_1$  ( $B_1$ ) and pass the signals from driver  $B_1$  ( $A_1$ ).



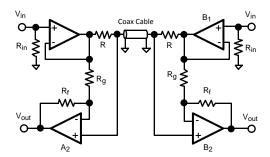


Figure 4. Circuit in Which One of the LMH6628's Amps is Used as a "Driver" and the Other as a Difference "Receiver" Amplifier

The output of the receiver amplifier will be:

$$V_{out_{A(B)}} = \frac{1}{2} V_{in_{A(B)}} \left[ 1 - \frac{R_f}{R_g} \right] + \frac{1}{2} V_{in_{B(A)}} \left[ 1 + \frac{R_f}{R_g} \right]$$
(3)

Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of Figure 5 shows the simultaneous reception of signals transmitted at 1MHz and 10MHz.

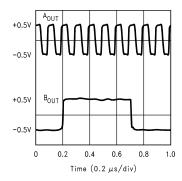


Figure 5. Simultaneous Reception of Signals Transmitted at 1MHz and 10MHz

### **POSITIVE PEAK DETECTOR**

The LMH6628's dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in Figure 6.

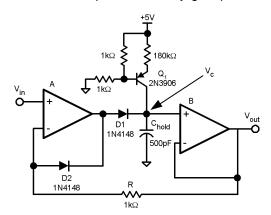


Figure 6. LMH6628's Dual Amplifiers Used to Implement a Unity-Gain Peak Detector Circuit

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging  $C_{hold}$ . A plot of the circuit's performance is shown in Figure 7 with a 1MHz sinusoidal input.

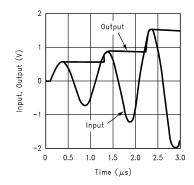


Figure 7. Circuit's Performance With a 1MHz Sinusoidal Input

A current source, built around Q1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D2 prevents negative saturation when  $V_{IN}$  is less than  $V_{C}$ . A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

#### ADJUSTABLE OR BANDPASS EQUALIZER

A "boost" equalizer can be made with the LMH6628 by summing a bandpass response with the input signal, as shown in Figure 8.

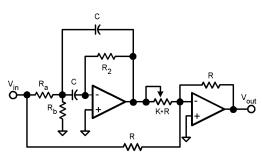


Figure 8. "Boost" Equalizer Made With the LMH6628 by Summing a Bandpass Response With the Input Signal

The overall transfer function is shown in Equation 4.

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \left[\frac{R_b}{K(R_a + R_b)}\right] \frac{s2Q\omega_o}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} - 1$$
(4)

To build a boost circuit, use the design equations Equation 5 and Equation 6.

$$\frac{R_2C}{2} = \frac{Q}{\omega_0} \tag{5}$$

2C 
$$(R_a||R_b) = \frac{1}{Q\omega_o}$$
 (6

Select  $R_2$  and C using Equation 5. Use reasonable values for high frequency circuits -  $R_2$  between  $10\Omega$  and  $5k\Omega$ , C between 10pF and 2000pF. Use Equation 6 to determine the parallel combination of  $R_a$  and  $R_b$ . Select  $R_a$  and  $R_b$  by either the  $10\Omega$  to  $5k\Omega$  criteria or by other requirements based on the impedance  $V_{in}$  is capable of driving. Finish the design by determining the value of K from Equation 7 .

Peak Gain = 
$$\frac{V_{\text{out}}}{V_{\text{in}}} (\omega_{\text{o}}) = \frac{R_2}{2KR_a} - 1$$
 (7)



Figure 9 shows an example of the response of the circuit of Figure 8, where  $f_o$  is 2.3MHz. The component values are as follows:  $R_a$ =2.1k $\Omega$ ,  $R_b$  = 68.5 $\Omega$ ,  $R_2$  = 4.22k $\Omega$ , R = 500 $\Omega$ , KR = 50 $\Omega$ , C = 120pF.

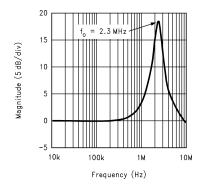


Figure 9. Example of Response of Circuit of Figure 8, Where fo is 2.3MHz

17-Nov-2012

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	_	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Samples
	(1)		Drawing			(2)		(3)	(Requires Login)
LMH6628MA	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	
LMH6628MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMH6628MAX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LMH6628MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6628MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6628MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6628MAX	SOIC	D	8	2500	349.0	337.0	45.0
LMH6628MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

# D (R-PDSO-G8)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



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