LMP8350 Ultra Low Distortion Fully Differential Precision ADC Driver with Selectable Power Modes

Check for Samples: LMP8350

FEATURES

- **Differential Input and Output**
- **Tri-Level Power Settings with Shutdown**
- **Ultra Low HD2/HD3 and THD+N Distortion**
- **Adjustable Output Common Mode Level**
- **Fully Balanced Differential Architecture**
- **Single or Dual Supply Operation**

APPLICATIONS

- **High Resolution Differential ADC Driver**
- **Portable instrumentation**
- **Precision Line Driver**

DESCRIPTION

The LMP8350 is an ultra low distortion fully differential amplifier designed for driving high-performance precision analog-to-digital converters (ADC). As part of the PowerWise™ family, a unique mode enable pin allows the user to choose from three different operating modes, trading power consumption for dynamic performance.

The high power mode is optimized for highest AC performance. The low noise, wide bandwidth and fast slew rate makes the LMP8350 ideal for driving 24bit ADCs with input sampling rates of 10MHz or less. The medium power mode is optimized for precision DC performance, and can be used to drive 24-bit ADCs with input sampling rates of 6MHz or less. The low power mode is a trade-off between AC performance and quiescent current for power sensitive applications. The disable mode fully shuts-down the amplifier for further standby power savings.

The fully differential architecture of this device allows for easy implementation of a single-ended to fully-differential output conversion. Driving a 3Vpp, 1kHz output sine wave with the amplifier powered by ±3.3V rails in high power mode yields 0.000098% THD+N.

The LMP8350 is part of the LMP™ precision amplifier family. It is offered in the 8-Pin SOIC package and has an operating temperature range of −40°C to +85°C.

Table 1. Key Specifications

	VALUE	UNIT
(T_A = 25°C, V_S = +10V, R_L = 2kΩ//20pF, typical values unless otherwise specified)		
Operating voltage range	4.5V to 12	V
Supply current	3 to 13mA	
Total THD+N @ 1KHz	0.000097%	
HD2 / HD3 Distortion @ 1KHz	< –124	dBc
Bandwidth	118	MHz
Settling to 0.1%	20 ns	
Low Offset Drift	0.4 µV/°C	
Offset Voltage	80µV	
Voltage Noise	4.6 nV/Hz	
Operating temperature range	−40°C to +85°C	

Typical Application

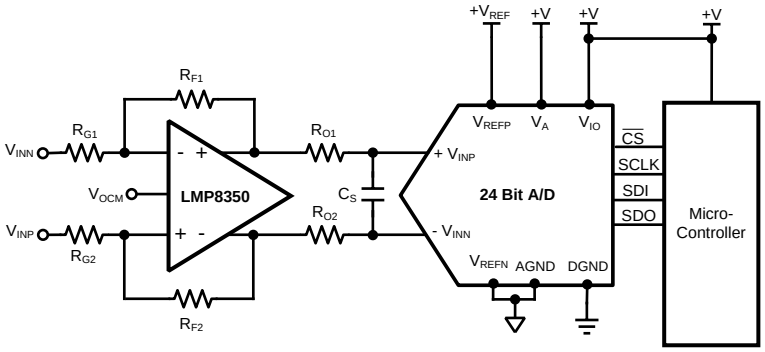


Figure 1. Typical Application Circuit

Connection Diagram

8-Pin SOIC

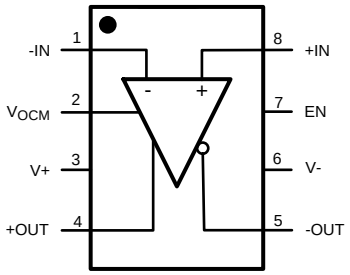


Figure 2. Top View

Table 2. Pin Descriptions

Pin	Name	Description
1	-IN	Inverting Input
2	V_{OCM}	Output Common Mode voltage set input. Sets output common mode voltage equal to the applied V_{OCM} pin voltage.
3	V+	Positive Power Supply Voltage
4	+OUT	Non-Inverting Output
5	-OUT	Inverting Output
6	V-	Negative Power Supply Voltage
7	EN	Enable and Power Select input. Applied voltage sets power level or shutdown mode.
8	+IN	Non-Inverting Input

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Human Body Model	2500 V
Machine Model	200V
Charge-Device Model	1250V
Output Short Circuit Duration	(3)
V+ relative to V-	-0.3 to +12.9V
IN+, IN-, OUT, EN and V_{OCM} Pins	V+ + 0.3V, V- – 0.3V
Input Current	1 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature (4)	+150°C

For soldering specifications:
See product folder at www.national.com and
www.national.com/ms/MS/MS-SOLDERING.pdf

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) The short circuit test is a momentary test which applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can exceed the maximum allowable junction temperature of 150°C. Positive number (+) is sourcing, negative number (-) is sinking.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings (1)

Temperature Range (T_A)	−40°C to +85°C
Supply Voltage ($V_S = V^+ – V^–$)	4.5V to 12V
Package Thermal Resistance (θ_{JA}) (2)	
8-Pin SOIC	150°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

+10V Electrical Characteristics (1)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Avcl = +1, R_F = R_G = 1kΩ, Fully differential input, V_S = +10V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM}=mid supply and HP mode unless otherwise noted. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions (2)	Min (3)	Typ (4)	Max (3)	Units
10V DC Characteristics						
V_{OS}	Input Offset Voltage (RTI)	High Power		±0.6	±4 **±4.05**	mV
		Mid Power		±0.08	±2 **±2.03**	
		Low Power		±0.1	±2.5 **±2.52**	
TCV_{OS}	Input Offset Voltage vs.Temperature (5)	High Power		±0.8		µV/°C
		Mid Power		±0.5		
		Low Power		±0.4		
I_B	Input Bias Current	High Power			2 **2.1**	µA
		Mid Power			2.7 **3.2**	
		Low Power			3.5 **3.7**	
A_{VOL}	Open Loop Gain	High Power	65	90		dB
		Mid Power	72	130		
		Low Power	74	114		
CMVR	Common Mode Voltage Range (6)	HP @ CMRR ≥73dB	1.2		8.8	V
		MP @ CMRR ≥83dB	1.2		8.8	
		LP @ CMRR ≥77dB	1.2		8.8	
CMRR	Common Mode Rejection Ratio	DC, V_{OCM}=0,VID=0, ΔVcm=±0.2V High Power	75	90		dB
		Medium Power	84	130		
		Low Power	79	114		
Z_{IND}	Differential Input Resistance	V_{CM} = mid supply		0.48		MΩ
C_{IND}	Differential Input Capacitance	V_{CM} = mid supply		1		pF
V_O	Output Swing (Single Ended)	High Power	0.86	0.75 to 9.25	9.14	V
		Mid Power	0.85	0.74 to 9.26	9.15	
		Low Power	0.86	0.81 to 9.19	9.14	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A

(2) For annotation brevity, “HP”=High Power, “MP”=Medium Power, “LP” =Low Power, “DIS”=Disabled or shut down, “SE”=Single Ended Mode, “DM”=Differential Mode. See table 1 in Applications section for power setting details. It is also assumed R_G = R_{G1} = R_{G2}

(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(5) Drift Determined by dividing the change in parameter at temperature extremes by the total temperature change. Value is the worst case of Ta_{MIN} to 25°C and 25°C to Ta_{MAX}.

(6) At amplifier inputs.

+10V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Avcl = +1, R_F = R_G = 1kΩ, Fully differential input, V_S = +10V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM}=mid supply and HP mode unless otherwise noted. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions (2)	Min (3)	Typ (4)	Max (3)	Units
I_{SHORT}	Short-Circuit Current	Output Shorted to mid supply (7)				mA
		High Power	+75 / -36	+108 / -65		
		Medium Power	+60 / -26	+85 / -48		
		Low Power	+15 / -6	+36 / -20		
PSRR	Power Supply Rejection Ratio V_S ±10%	High Power		107		dB
		Mid Power		118		
		Low Power		124		
I_S	Supply Current	V_{EN}=8.75 (8)		15	18 **20**	mA
		V_{EN}=6.25 (8)		8	10 **11**	
		V_{EN}=3.75 (8)		3	4 **5**	
PD	Power Down Mode	Disable Voltage Threshold (8)		<1.65		V
		Shutdown Current		0.75	0.9 **0.95**	mA
		Enable Pin Current		100		µA
t_{en}	Enable Time	High Power		15		ns
		Mid Power		20		
		Low Power		40		
10V AC Characteristics						
SSBW	Small Signal Bandwidth 200mVp-p Differential	High Power		118		MHz
		Mid Power		87		
		Low Power		31		
SR	Slew Rate 2Vp-p Differential (9)	High Power		507		V/µs
		Mid Power		393		
		Low Power		178		
t_{rise}	Rise Time 2Vp-p Differential	High Power		3.0		ns
		Mid Power		3.9		
		Low Power		9.7		
t_{fall}	Fall Time 2Vp-p Differential	High Power		2.8		ns
		Mid Power		3.8		
		Low Power		9.6		
t_s	0.1% Settling Time 2Vp-p	2V Step, C_L = 20pF High Power		20		ns
		Mid Power		25		
		Low Power		38		
e_n	Input Referred Voltage Noise @ 10KHz	High Power		4.6		$nV/\sqrt{Hz}$
		Mid Power		4.8		
		Low Power		8		

(7) The short circuit test is a momentary test which applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can exceed the maximum allowable junction temperature of 150°C. Positive number (+) is sourcing, negative number (-) is sinking.
(8) Enable voltage is referred to V- (negative supply voltage).
(9) Slew Rate is the average of the rising and falling edges.

+10V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Avcl = +1, R_F = R_G = 1kΩ, Fully differential input, V_S = +10V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM}=mid supply and HP mode unless otherwise noted. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions (2)	Min (3)	Typ (4)	Max (3)	Units
I_n	Input Referred Current Noise @ 10KHz	f = 10 kHz High Power		1.7		pA/√Hz
		Mid Power		1.1		
		Low Power		0.6		
THD+N	Total Harmonic Distortion + Noise 3Vp-p @ 1KHz	High Power		0.000097		%
		Mid Power		0.000109		
		Low Power		0.000185		
HD2	2nd Harmonic Distortion 3Vp-p, 1KHz	High Power		–124.7	–116	dBc
		Mid Power		–122.8		
		Low Power		–117.2		
	2nd Harmonic Distortion 6Vp-p, 1KHz	High Power		–118.9		dBc
		Mid Power		–117.6		
		Low Power		–114.7		
HD3	3rd Harmonic Distortion 3Vp-p, 1KHz	High Power		–139.9	–126	dBc
		Mid Power		–141.9		
		Low Power		–133.3		
	3rd Harmonic Distortion 6Vp-p, 1KHz	High Power		–129.5		dBc
		Mid Power		–132.4		
		Low Power		–129.4		
10V V_{OCM} Input Characteristics						
	V_{OCM} Small Signal Bandwidth 200mVp-p	High Power		4.8		MHz
		Mid Power		2.4		
		Low Power		0.64		
	V_{OCM} Gain			1		V/V
	V_{OCM} Offset Voltage	High Power		±1.62		mV
		Mid Power		±0.23		
		Low Power		±0.43		
	V_{OCM} Voltage Range	All Power Levels		1.8 to 8.2		V
	V_{OCM} Input Resistance	All power levels		30 to mid supply		KΩ

+6.6V Electrical Characteristics (1)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Avcl = +1, R_F = R_G = 1kΩ, Fully differential input, V_S = +6.6V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM}=mid supply and HP mode unless otherwise noted. **Boldface** limits apply at the temperature extremes..

Symbol	Parameter	Conditions (2)	Min (3)	Typ (4)	Max (3)	Units
6.6V DC Characteristics						
V_{OS}	Input Offset Voltage (RTI)	High Power		±0.3	±3.5 **±3.54**	mV
		Mid Power		±0.1	±2.8 **±2.83**	
		Low Power		±0.1	±2.5 **±2.52**	
TCV_{OS}	Input Offset Voltage vs.Temperature (5)	High Power		±0.7		µV/°C
		Mid Power		±0.5		
		Low Power		±0.4		
I_B	Input Bias Current	High Power			1.4 **2.4**	µA
		Mid Power			2.5 **3.0**	
		Low Power			3.5 **3.7**	
A_{VOL}	Open Loop Gain	High Power	65	70		dB
		Mid Power	73	76		
		Low Power	72	75		
CMVR	Common Mode Voltage Range (6)	HP @ CMRR ≥68dB	1.2		5.4	V
		MP @ CMRR ≥63dB	1.2		5.4	
		LP @ CMRR ≥ 79dB	1.2		5.4	
CMRR	Common Mode Rejection Ratio	DC, V_{OCM}=0,VID=0, ΔVcm=±0.2V High Power	70	85		dB
		Mid Power	86	117		
		Low Power	81	113		
Z_{IND}	Differential Input Resistance	V_{CM} = mid supply		0.48		MΩ
C_{IND}	Differential Input Capacitance	V_{CM} = mid supply		1		pF
V_O	Output Swing (Single Ended)	High Power	0.84	0.77 to 5.83	5.76	V
		Mid Power	0.82	0.75 to 5.83	5.78	
		Low Power	0.83	0.77 to 5.83	5.77	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A

(2) For annotation brevity, “HP”=High Power, “MP”=Medium Power, “LP” =Low Power, “DIS”=Disabled or shut down, “SE”=Single Ended Mode, “DM”=Differential Mode. See table 1 in Applications section for power setting details. It is also assumed R_G = R_{G1} = R_{G2}

(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(5) Drift Determined by dividing the change in parameter at temperature extremes by the total temperature change. Value is the worst case of Ta_{MIN} to 25°C and 25°C to Ta_{MAX}.

(6) At amplifier inputs.

+6.6V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Avcl = +1, R_F = R_G = 1kΩ, Fully differential input, V_S = +6.6V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM}=mid supply and HP mode unless otherwise noted. **Boldface** limits apply at the temperature extremes..

Symbol	Parameter	Conditions (2)	Min (3)	Typ (4)	Max (3)	Units
I_{SHORT}	Short-Circuit Current	Output Shorted to mid supply (7)				mA
		High Power	+54 / –30	+83 / –49		
		Mid Power	+40 / –19	+64 / –35		
		Low Power	+15 / –6	+27 / –15		
PSRR	Power Supply Rejection Ratio V_S ±10%	High Power		111		dB
		Mid Power		117		
		Low Power		127		
I_S	Supply Current	V_{EN}=5.775 (8)		14	16 **18**	mA
		V_{EN}=4.125 (8)		7	9 **10**	
		V_{EN}=2.475 (8)		2	3 **4**	
PD	Power Down Mode	Disable Voltage Threshold (8)		<1.225		V
		Shutdown Current		0.55	0.65 **0.7**	mA
		Enable Pin Current		40		µA
t_{en}	Enable Time	High Power		18		ns
		Mid Power		22		
		Low Power		43		
6.6V AC Characteristics						
SSBW	Small Signal Bandwidth 200mVp-p Differential	High Power		116		MHz
		Mid Power		85		
		Low Power		29		
SR	Slew Rate 2Vp-p Differential (9)	High Power		488		V/µs
		Mid Power		376		
		Low Power		166		
t_{rise}	Rise Time 2Vp-p Differential	High Power		3.1		ns
		Mid Power		4.2		
		Low Power		10.4		
t_{fall}	Fall Time 2Vp-p Differential	High Power		3.0		ns
		Mid Power		4.0		
		Low Power		10.3		
t_s	0.1% Settling Time 2Vp-p	2V Step, C_L = 20pF High Power		19		ns
		Mid Power		25		
		Low Power		43		
e_n	Input Referred Voltage Noise @ 10KHz	High Power		4.5		$nV/\sqrt{Hz}$
		Mid Power		4.8		
		Low Power		8		

(7) The short circuit test is a momentary test which applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can exceed the maximum allowable junction temperature of 150°C. Positive number (+) is sourcing, negative number (-) is sinking.
(8) Enable voltage is referred to V- (negative supply voltage).
(9) Slew Rate is the average of the rising and falling edges.

+6.6V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Avcl = +1, R_F = R_G = 1kΩ, Fully differential input, V_S = +6.6V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM}=mid supply and HP mode unless otherwise noted. **Boldface** limits apply at the temperature extremes..

Symbol	Parameter	Conditions (2)	Min (3)	Typ (4)	Max (3)	Units
I_n	Input Referred Current Noise @ 10KHz	High Power		1.7		pA/√Hz
		Mid Power		1.2		
		Low Power		0.6		
THD+N	Total Harmonic Distortion + Noise 3Vp-p @ 1KHz	High Power		0.000098		%
		Mid Power		0.00011		
		Low Power		0.000089		
HD2	2nd Harmonic Distortion 3Vp-p, 1KHz	High Power		–124.7		dBc
		Mid Power		–122.8		
		Low Power		–117.2		
	2nd Harmonic Distortion 6Vp-p, 1KHz	High Power		–118.9		dBc
		Mid Power		–117.6		
		Low Power		–114.7		
HD3	3rd Harmonic Distortion 3Vp-p, 1KHz	High Power		–139.9		dBc
		Mid Power		-141.9		
		Low Power		–133.3		
	3rd Harmonic Distortion 6Vp-p, 1KHz	High Power		–121.4		dBc
		Mid Power		–125.3		
		Low Power		–124.5		
6.6V V_{OCM} Input Characteristics						
	V_{OCM} Small Signal Bandwidth 200mVp-p	High Power		4.5		MHz
		Mid Power		2.2		
		Low Power		0.6		
	V_{OCM} Gain			1		V/V
	V_{OCM} Offset Voltage	High Power		±0.97		mV
		Mid Power		±0.43		
		Low Power		±0.89		
	V_{OCM} Voltage Range	All Power Levels		1.2 to 5.4		V
	V_{OCM} Input Resistance	All power levels		30 to mid supply		KΩ

+5V Electrical Characteristics (1)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Avcl = +1, R_F=R_G = 1kΩ, Fully differential input, V_S = +5V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM}=mid supply and HP mode unless otherwise noted. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
5V DC Characteristics						
V_{OS}	Input Offset Voltage (RTI)	High Power		±0.2	±3.2 **±3.6**	mV
		Mid Power		±0.1	±2.0 **±2.3**	
		Low Power		±0.1	±2.0 **±2.3**	
TCV_{OS}	Input Offset Voltage vs.Temperature (4)	High Power		±0.7		µV/°C
		Mid Power		±0.5		
		Low Power		±0.4		
I_B	Input Bias Current	High Power			1.5 **1.6**	µA
		Mid Power			2.5 **3.0**	
		Low Power			3.5 **3.7**	
A_{VOL}	Open Loop Gain	High Power	63	68		dB
		Mid Power	71	75		
		Low Power	68	75		
CMVR	Common Mode Voltage Range (5)	HP @ CMRR ≥60dB	1.15		3.85	V
		MP @ CMRR ≥86dB	1.15		3.85	
		LP @ CMRR ≥80dB	1.15		3.85	
CMRR	Common Mode Rejection Ratio	DC, V_{OCM}=0,VID=0, ΔVcm=±0.2V High Power	63	79		dB
		Mid Power	87	114		
		Low Power	82	114		
Z_{IND}	Differential Input Resistance	V_{CM} = mid supply		0.48		MΩ
C_{IND}	Differential Input Capacitance	V_{CM} = mid supply		1		pF
V_O	Output Swing (Single Ended)	High Power	0.82	0.77 to 4.23	4.18	V
		Mid Power	0.82	0.75 to 4.25	4.18	
		Low Power	0.83	0.77 to 4.23	4.17	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(4) Drift Determined by dividing the change in parameter at temperature extremes by the total temperature change. Value is the worst case of Ta_{MIN} to 25°C and 25°C to Ta_{MAX}.

(5) At amplifier inputs.

+5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Avcl = +1, R_F=R_G = 1kΩ, Fully differential input, V_S = +5V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM}=mid supply and HP mode unless otherwise noted. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
I_{SHORT}	Short-Circuit Current	Output Shorted to mid supply (6)				mA
		High Power	+44 / –25	+72 / –42		
		Mid Power	+34 / –16	+57 / –31		
		Low Power	+12 / –5	+23 / –13		
PSRR	Power Supply Rejection Ratio V_S ±10%	High Power		117		dB
		Mid Power		120		
		Low Power		111		
I_S	Supply Current	V_{EN}=4.375 (7)		13	15 **17**	mA
		V_{EN}=3.125 (7)		7	9 **10**	
		V_{EN}=1.875 (7)		2	3 **4**	
PD	Power Down Mode	Disable Voltage Threshold (7)		<1.025		V
		Shutdown Current		0.50	0.85 **0.90**	mA
		Enable Pin Current		15		µA
t_{en}	Enable Time	High Power		20		ns
		Mid Power		22		
		Low Power		50		
5V AC Characteristics						
SSBW	Small Signal Bandwidth 200mVp-p Differential	High Power		114.5		MHz
		Mid Power		84		
		Low Power		28		
SR	Slew Rate 2Vp-p Differential (8)	High Power		476		V/µs
		Mid Power		366		
		Low Power		160		
t_{rise}	Rise Time 2Vp-p Differential	High Power		3.2		ns
		Mid Power		4.3		
		Low Power		10.8		
t_{fall}	Fall Time 2Vp-p Differential	High Power		3.1		ns
		Mid Power		4.1		
		Low Power		10.7		
t_s	0.1% Settling Time 2Vp-p	2V Step, C_L = 20pF High Power		19		ns
		Mid Power		24		
		Low Power		48		
e_n	Input Referred Voltage Noise	f = 10 kHz High Power		4.5		$nV/\sqrt{Hz}$
		Mid Power		4.8		
		Low Power		8		

(6) The short circuit test is a momentary test which applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can exceed the maximum allowable junction temperature of 150°C. Positive number (+) is sourcing, negative number (-) is sinking.
(7) Enable voltage is referred to V- (negative supply voltage).
(8) Slew Rate is the average of the rising and falling edges.

+5V Electrical Characteristics (1) (continued)

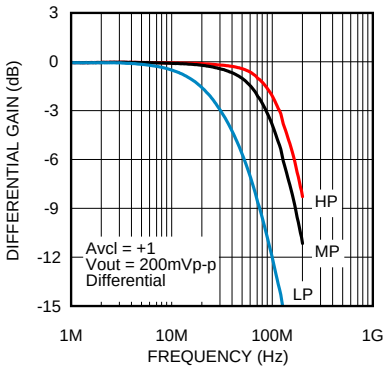
Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Avcl = +1, R_F=R_G = 1kΩ, Fully differential input, V_S = +5V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM}=mid supply and HP mode unless otherwise noted. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
I_n	Input Referred Current Noise	f = 10 kHz High Power		1.8		pA/√Hz
		Mid Power		1.2		
		Low Power		0.6		
THD+N	Total Harmonic Distortion + Noise 3Vp-p @ 1KHz	High Power		0.000107		%
		Mid Power		0.000114		
		Low Power		0.000192		
HD2	2nd Harmonic Distortion 3Vp-p, 1KHz	High Power		–125.3		dBc
		Mid Power		–122.6		
		Low Power		–117.0		
HD3	3rd Harmonic Distortion 3Vp-p, 1KHz	High Power		–125.5		dBc
		Mid Power		–130.0		
		Low Power		–128.7		
5V V_{OCM} Input Characteristics						
	V_{OCM} Small Signal Bandwidth 200mVp-p	High Power		4.4		MHz
		Mid Power		2.2		
		Low Power		0.56		
	V_{OCM} Gain			1		V/V
	V_{OCM} Offset Voltage	High Power		±0.46		mV
		Mid Power		±0.53		
		Low Power		±0.11		
	V_{OCM} Voltage Range	All Power Levels		1.15 to 3.85		V
	V_{OCM} Input Resistance	All power levels		30 to mid supply		KΩ

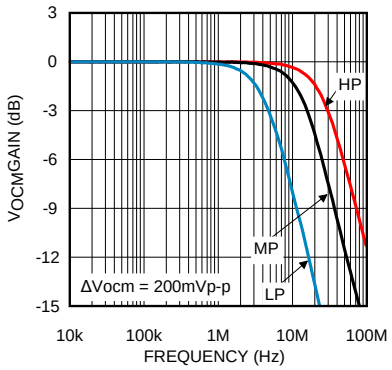
Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, Avcl = +1, R_F=R_G = 1kΩ, fully differential input, V_S = +10V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM} = mid supply and HP mode unless otherwise noted.

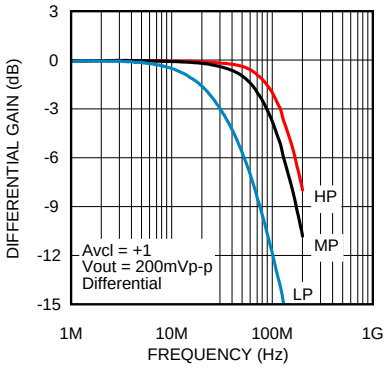
Frequency Response at 10V



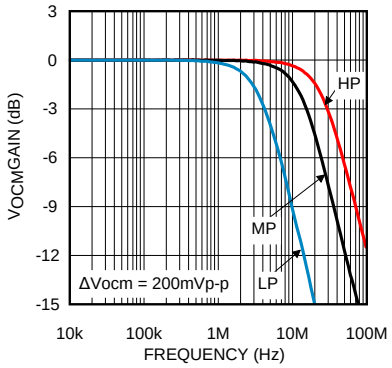
V_{OCM} Frequency Response at 10V



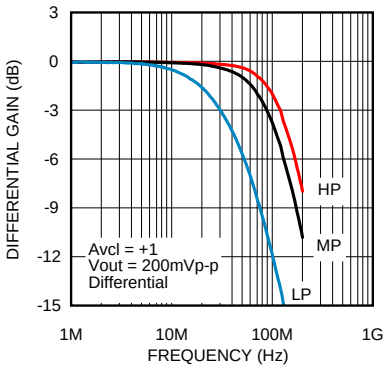
Frequency Response at 6.6V



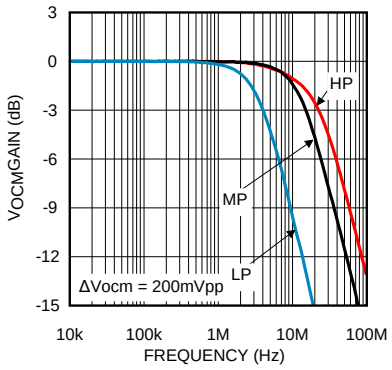
V_{OCM} Frequency Response at 6.6V



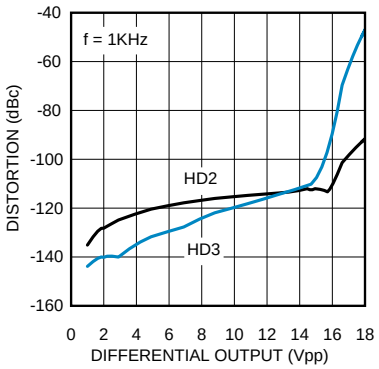
Frequency Response at 5V



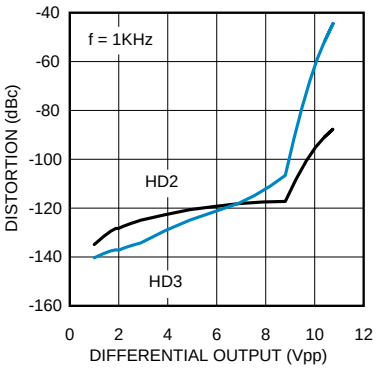
V_{OCM} Frequency Response at 5V



Distortion at 10V, High Power



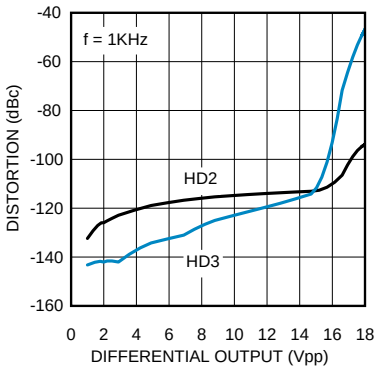
Distortion at 6.6V, High Power



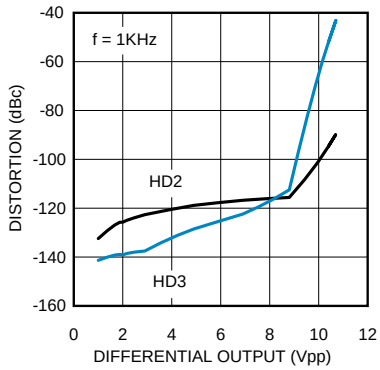
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, Avcl = +1, R_F=R_G = 1kΩ, fully differential input, V_S = +10V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM} = mid supply and HP mode unless otherwise noted.

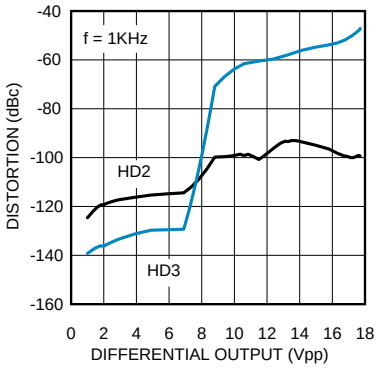
Distortion at 10V, Mid Power



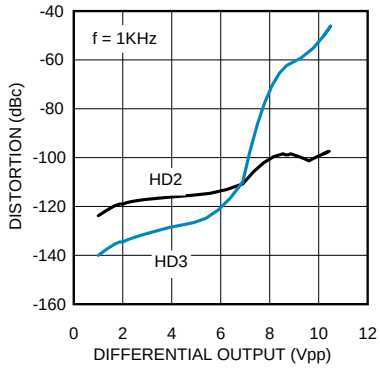
Distortion at 6.6V, Mid Power



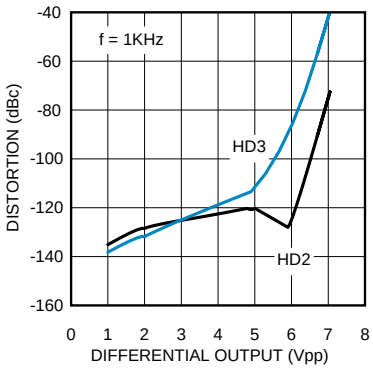
Distortion at 10V, Low Power



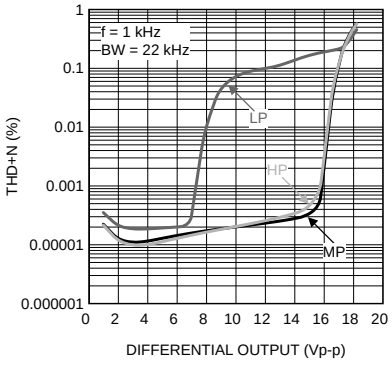
Distortion at 6.6V, Low Power



Distortion at 5V, High Power



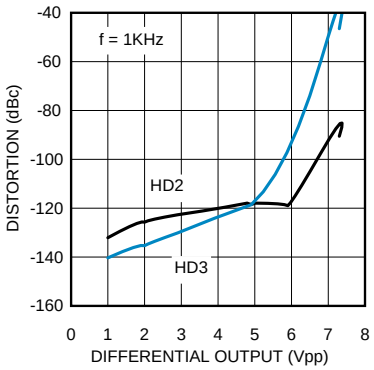
THD+N at 10V



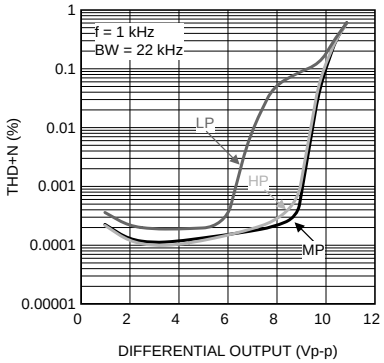
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, Avcl = +1, R_F=R_G = 1kΩ, fully differential input, V_S = +10V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM} = mid supply and HP mode unless otherwise noted.

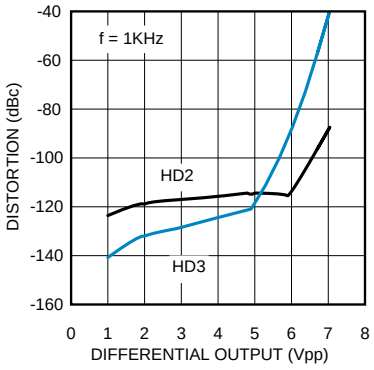
Distortion at 5V, Mid Power



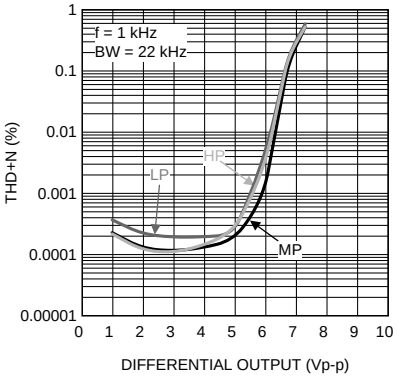
THD+N at 6.6V



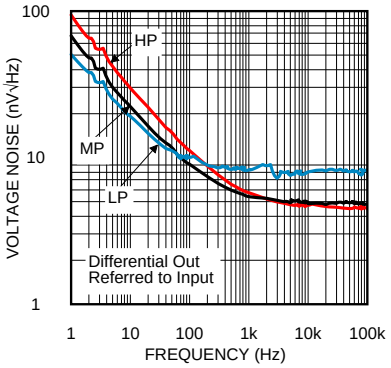
Distortion at 5V, Low Power



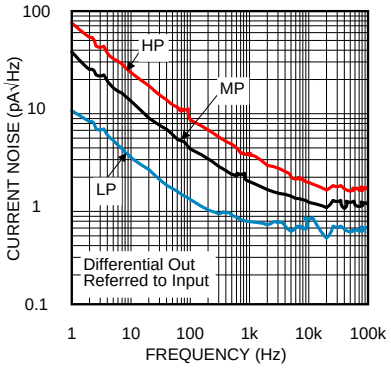
THD+N at 5V



Voltage Noise at 10V



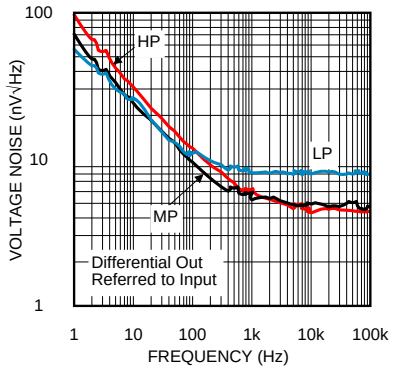
Current Noise at 10V



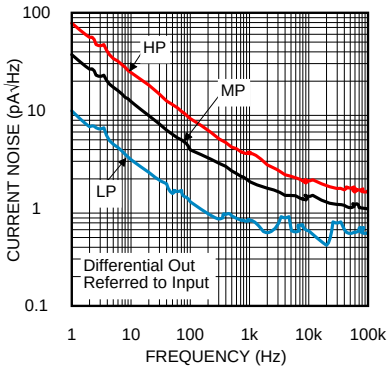
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, Avcl = +1, R_F=R_G = 1kΩ, fully differential input, V_S = +10V, R_L = 2 kΩ//20pF differentially, Input CMR and V_{OCM} = mid supply and HP mode unless otherwise noted.

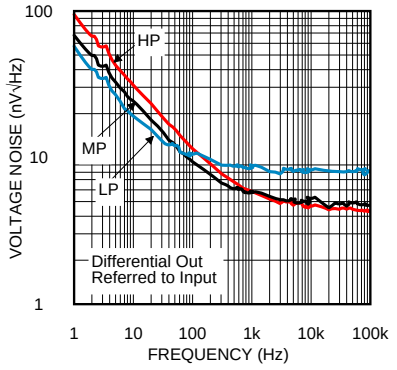
Voltage Noise at 6.6V



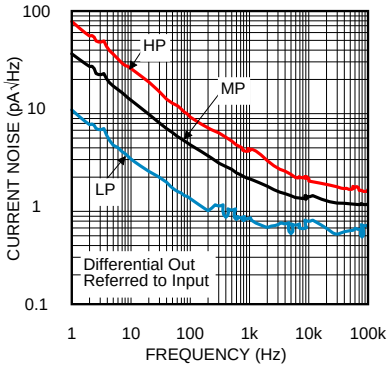
Current Noise at 6.6V



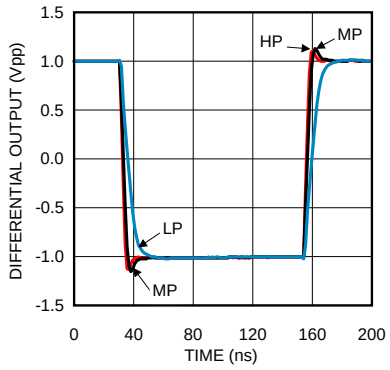
Voltage Noise at 5V



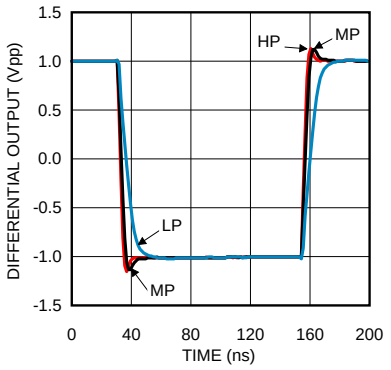
Current Noise at 5V



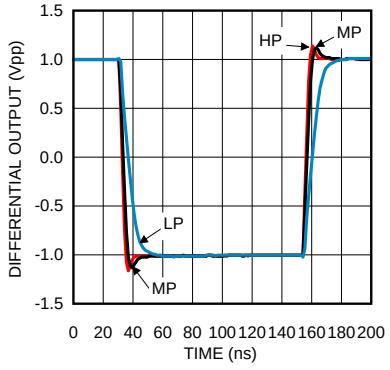
Pulse Response at 10V



Pulse Response at 6.6V



Pulse Response at 5V



Application Section

The LMP8350 is a fully differential voltage feedback amplifier designed to drive precision differential ADC converters. The LMP8350, though fully integrated for ultimate balance and distortion performance, functionally provides three channels. Two of these channels are the V^+ and V^- signal path channels, which function similarly to inverting mode operational amplifiers and are the primary signal paths.

The third "channel" is the common mode (V_{OCM}) feedback circuit. This is the circuit that sets the output common mode as well as driving the V^+ and V^- outputs to be equal magnitude and opposite phase, even when only one of the two input channels is driven. The common mode feedback circuit allows for single ended to differential operation. The output common mode voltage is set by applying the appropriate voltage to the V_{OCM} pin.

ENABLE PIN AND POWER MODE SELECTION

The LMP8350 is equipped with a four level enable (EN) pin to select one of three power modes or shutdown. These modes are selected by applying the appropriate voltage to the EN pin.

Each power level has a corresponding performance level. The high power mode will have the best overall BW and distortion performance, but at the cost of higher supply current and some DC accuracy. The Low power mode has the lowest supply current, but with a noticeable loss of AC performance and output drive capabilities. The mid-power mode provides the best balance of AC and precision DC specifications. In disable mode, the amplifier is shutdown and the output stage goes into a high impedance state. Table 3 summarizes these performance trade-offs.

Table 3. Performance vs. Power Mode Summary

Mode	V_S	–3dB BW (MHz)	HD2 (dBc)	Noise (nV/Hz)	SR (V/µS)	Typ Vos (mV)
High	10	118	–124.7	4.6	507	0.6
	6.6	116	–124.7	4.5	488	0.3
	5	114	–125.5	4.5	476	0.2
Med	10	87	–122.8	4.8	393	0.08
	6.6	85	–122.8	4.8	376	0.1
	5	84	–122.6	4.8	366	0.1
Low	10	31	–117.2	8.0	178	0.1
	6.6	29	–117.2	8.0	166	0.1
	5	28	–117.0	8.0	160	0.1

To set the mode, internally the voltage at the EN pin is compared against the total supply voltage (V_S) and sets the current consumption as shown in the table below. The EN pin voltage is referenced to the V- pin.

Table 4. Enable Pin Mode Selection

V_{EN} (V_S = V+ - V-)	Power Mode	V_{EN} @ 10V	V_{EN} @ 6.6V	V_{EN} @ 5V	I_S mA
7/8 * V_S	High	8.75	5.775	4.375	13 to 15
5/8 * V_S	Med	6.25	4.125	3.125	7 to 9
3/8 * V_S	Low	3.75	2.475	1.875	2 to 3
1/8 * V_S	Dis	1.25	0.825	0.625	<1

The enable pin should not be allowed to float. If the enable pin is not used it can be tied to V+ to select the high power mode or set with two resistors.

Each power setting has a +/-400mV tolerance at each level, though it is recommended to keep the set voltage within the center of the range as performance may vary near the transition zones.

During shutdown, both outputs are in a high impedance state, so the feedback and gain set resistors will then set the input and output impedance of the circuit. For this reason input to output isolation will be poor in the disabled state.

The voltage at the EN pin can be generated with a resistive voltage divider or a buffer connected to a voltage source or a DAC. The schematic diagram below shows how to generate EN voltage with a resistive voltage divider.

Values of R_A and R_B can be calculated to achieve the voltages in Table 4, however their sum should be below 50kΩ to keep the voltage at the enable pin stable. Recommended values for Ra and Rb are given in Table 5.

Table 5. Recommended Ra and Rb for Mode Selection

Mode	10V	6.6V	5V	V_{EN}
High Power	R_A=0 R_B=inf	R_A=0 R_B=inf	R_A=0 R_B=inf	>7/8 V_S
Med Power	R_A=18K R_B=30K	R_A=18K R_B=30K	R_A=18K R_B=30K	5/8 V_S
Low Power	R_A=33K R_B=18K	R_A=33K R_B=18K	R_A=33K R_B=18K	3/8 V_S
Shutdown	R_A=Inf R_B=0	R_A=Inf R_B=0	R_A=Inf R_B=0	<1/8 V_S

V_{OCM} PIN AND OUTPUT COMMON MODE SETTING

Output common mode voltage is set by the V_{OCM} pin. Both outputs will be offset in the same direction (phase) by an amount equal to the applied V_{OCM} voltage.

The V_{OCM} pin, if left unconnected, will self-bias to mid-supply . Two internal 60KΩ resistors set this midpoint. These resistors are shown in Figure 3.

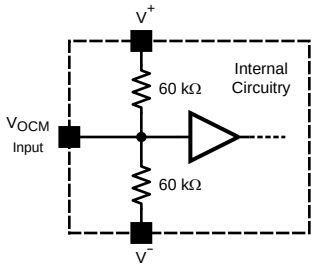


Figure 3. V_{OCM} Internal Bias Circuit

The equivalent resistance looking into the V_{OCM} pin will look like 30KΩ to mid supply, plus about ±700nA for internal base currents (which scales with power mode and supply current). If left floating, the V_{OCM} input should be bypassed to ground with a 0.1 µF ceramic capacitor.

If a different output common mode voltage is desired, the V_{OCM} pin should be driven by a clean, low impedance source to override the internal divider resistors. The V_{OCM} pin should be bypassed to ground with a 0.1 µF ceramic capacitor. It should be noted that any signal or noise coupling into the V_{OCM} will be passed as common mode noise and may result in the loss of dynamic range, degraded CMRR, degraded balance and higher distortion. The V_{OCM} pin is primarily intended as a DC bias path and is not intended for use as a signal path.

For applications that can tolerate slight shifts in the V_{OCM}voltage over temperature, it is also possible to use a single resistor to program the V_{OCM} voltage by paralleling one of the internal resistors to change the ratio.

FULL BANDWIDTH LIMITATIONS

Although the LMP8350 has a unity gain bandwidth of over 200MHz, it is primarily intended for lower sample rate, high-precision ADC's with baseband analog input signal bandwidths in the DC to <1MHz range (not to be confused with sampling rate). The LMP8350's high open loop bandwidth is used to provide ultra low-distortion and fast settling times. Maximum power bandwidth is limited by the internal output common mode feedback path, which is limited to 1MHz to 5MHz. Operation with input signals above 1MHz with near full output swings can cause random shifts in the output common mode and possible AC instabilities. For this reason, the LMP8350 is not intended to be used wide bandwidth (>1MHz) signal paths. Single ended inputs rely on the common mode signal path and will have a bandwidth limited to that of the internal common mode buffer.

FULLY DIFFERENTIAL OPERATION

The LMP8350 will perform best when used with split supplies and in a fully differential configuration. See Figure 4 for recommend circuits.

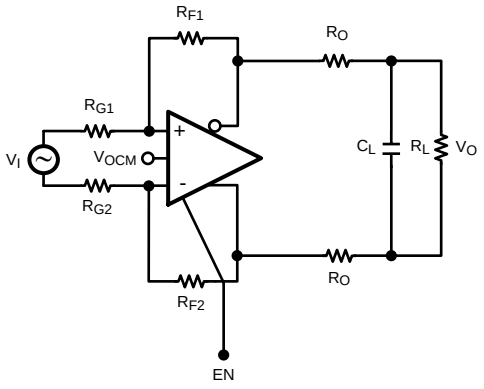


Figure 4. Typical Fully Differential Application

The circuit shown in Figure 4 is a typical fully differential application as might be used to drive a Sigma Delta ADC. In this circuit, closed loop gain, is (A_V) = V_{OUT}/ V_{IN} = R_F/R_G, where R_F=R_{F1}=R_{F2} and R_G=R_{G1}=R_{G2}. For all the applications in this data sheet , V_{IN} is presumed to be the voltage presented to the circuit by the signal source. For differential signals this will be the difference of the signals on each input (which will be double the magnitude of each individual signal), while in single ended inputs it will just be the driven input signal.

When fed with a differential signal, the LMP8350 provides excellent distortion, balance and common mode rejection, provided the resistors R_F, R_G and any input termination resistors (R_T) are well matched and strict symmetry is observed in board layout. With a DC CMRR of over 80 dB, the DC and low frequency CMRR of most circuits will be dominated by the external resistor matching and board trace resistance. At low distortion levels, board layout symmetry and supply bypassing become a factor as well. It is assumed throughout this document that R_{F1} = R_{F2} and R_{G1} = R_{G2} for maximum channel symmetry

Precision resistors of at least 0.1% accuracy or better are recommended and careful board layout will also be required for optimum performance.

Operation with R_F feedback resistors as low as 300 ohms is possible in the High and Medium power modes. This will slightly improve the noise and bandwidth results. However, feedback resistors with R_F values of less than 1KΩ should be avoided in the low power mode due to the reduced output drive current capabilities. If low value resistors (<300Ω) must be used in the low power mode, the maximum output swing will need to be limited.

The resistors R_O help keep the amplifier stable when presented with a load C_L, as is common when driving an analog to digital converter (ADC).

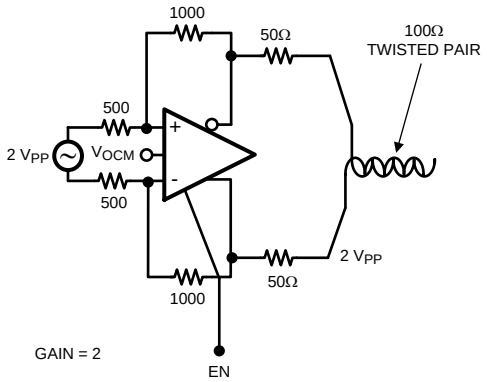
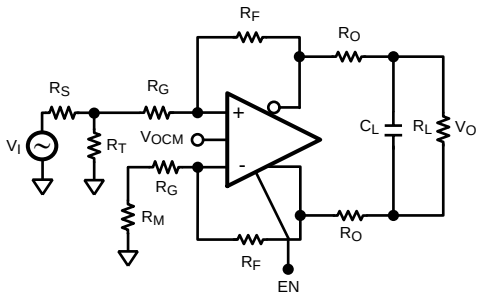


Figure 5. Fully Differential Cable Driver

With up to 15 V_{PP} differential output voltage swing and 80 mA of linear drive current, the LMP8350 makes an excellent precision cable driver as shown in Figure 5. The LMP8350 is also suitable for driving differential cables from a single ended source.



SET $R_M = R_T || R_S$

SET $R_T = \dfrac{1}{\left(\dfrac{1}{R_S} - \dfrac{1}{R_{IN}}\right)}$ $R_{IN} = \dfrac{R_G}{1 - \left(\dfrac{R_F}{2 * (R_F + R_G)}\right)}$

Figure 6. Single Ended in Differential Out

SINGLE ENDED INPUT TO DIFFERENTIAL OUTPUT

Figure 6 shows a typical application where an LMP8350 is used to produce a differential signal from a single ended source. It should be noted that compared to differential input, using a single ended input will reduce gain by 1/2, so that the closed loop gain will be; Gain = $A_V = 0.5 * R_F/R_G$.

In single ended input operation the output common mode voltage is set by the V_{OCM} pin. Also, In this mode the common mode feedback circuit must recreate the signal that is not present on the unused differential input pin. The common mode feedback circuit is responsible for ensuring balanced output with a single ended input.

Balance error is defined as the amount of input signal that couples into the output common mode. It is measured as the undesired output common mode swing divided by the signal on the input. Balance error can be caused by either a channel to channel gain error, or phase error. Either condition will produce a common mode shift. As mentioned in the previous FULL BANDWIDTH LIMITATIONS section, the overall bandwidth is limited due to the V_{OCM} buffer bandwidth limitations in this configuration.

Supply and V_{OCM} pin bypassing are also critical in this mode of operation.

SINGLE SUPPLY OPERATION

As shown in Figure 7, the input common mode voltage is less than the output common voltage. It is set by current flowing through the feedback network from the device output. The input common mode voltage range places constraints on gain settings. Possible solutions to this limitation include AC coupling the input signal, using split power supplies and limiting stage gain. AC coupling with single supply is shown in Figure 8.

V_{ICM}= Input common mode voltage = $(V^+_{IN}+V^-_{IN})/2$.

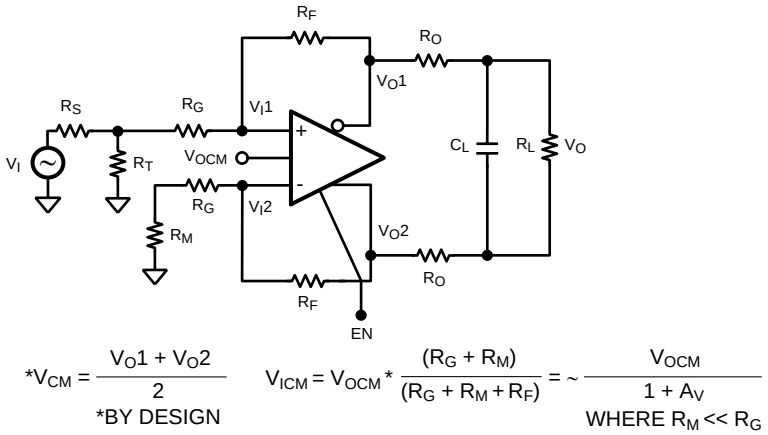


Figure 7. Relating A_V to Input/Output Common Mode Voltages

In Figure 7 the differential closed loop gain is = A_V= R_F/R_G. Please note that in single ended to differential operation V_{IN} is measured single ended while V_{OUT} is measured differentially. This means that gain is really one-half, or 6 dB, less when measured on either of the output pins separately.

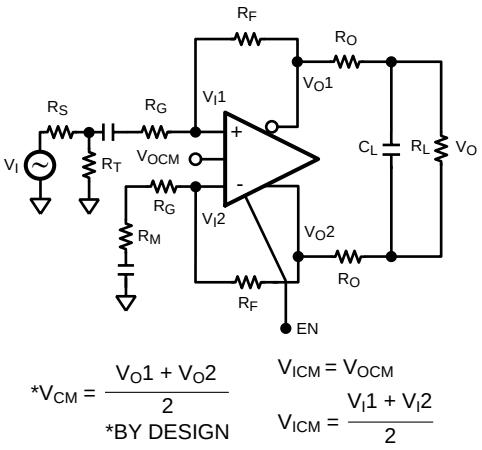


Figure 8. AC Coupled for Single Supply Operation

POWER SUPPLY AND V_{OCM} BYPASSING

The LMP8350 requires supply bypassing capacitors as shown in Figure 9 and Figure 10 for fastest settling time and overall stability.

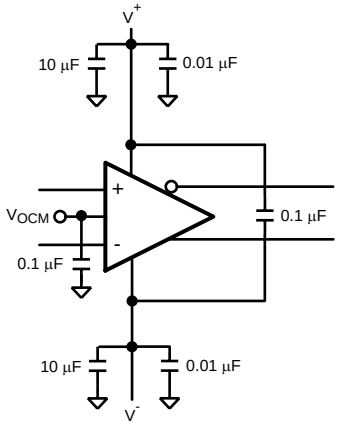


Figure 9. Split Supply Bypassing Capacitors

The 0.01 µF and 0.1 µF capacitors should be leadless surface mount (SMT) ceramic capacitors and should be no more than 3 mm from the supply pins. The SMT capacitors should be connected directly to a ground plane. Thin traces or small vias will reduce the effectiveness of bypass capacitors.

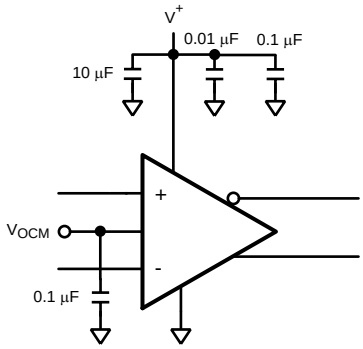


Figure 10. Single Supply Bypassing Capacitors

Also shown in both figures is a capacitor from the V_{OCM} pin to ground. The V_{OCM} pin sets the output common mode voltage. Any noise on this input is transferred directly to the output. The V_{OCM} pin should be bypassed even if the pin in not used. There is an internal resistive divider on chip to set the output common mode voltage to the mid point of the supply pins. The impedance looking into this pin is approximately 30 kΩ. If a different output common mode voltage is desired drive this pin with a clean, accurate voltage reference.

DRIVING ANALOG TO DIGITAL CONVERTERS

Analog to digital converters (ADC) present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. As well, there are usually current spikes associated with switched capacitor or sample and hold circuits. Figure 11 shows a typical circuit for driving an ADC. The two resistors serve to isolate the capacitive loading of the ADC from the amplifier and ensure stability. In addition, the resistors form part of a low pass filter which helps to provide anti alias and noise reduction functions. The C_S capacitor helps to smooth the current spikes associated with the internal switching circuits of the ADC and also are a key component in the low pass filtering of the ADC input. The capacitor should be a low distortion capacitor, such as an NPO, to avoid causing significant distortion terms. In the circuit of Figure 11, the cutoff frequency of the filter is $1/ (2*\pi*(R_{ISO1}+R_{ISO2}) *(C_S + C_{CONVERTER}))$, which should be slightly less than the sampling frequency. Note that the ADC input capacitance must be factored into the frequency response of the input filter. Also as shown in Figure 11, the input capacitance to many ADCs is variable based on the clock cycle. For lower speed, precision ADC's, the external cap is generally sized to ten times the internal sampling capacitor value. See the data sheet for your particular ADC for details.

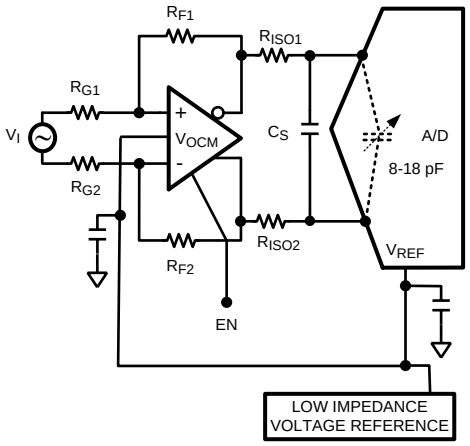


Figure 11. Driving an ADC

The amplifier and ADC should be located as close together as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on the output traces, and the ADC is sensitive to high frequency noise that may couple in on its input lines. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the Nyquist range (DC to Fs/2). See AN-236 for more details on the subsampling process and the requirements this imposes on the filtering necessary in your system.

CAPACITIVE DRIVE

As noted in the Driving ADC section, capacitive loads should be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500Ω or higher. A typical ADC has capacitive components of around 8 to 18pF, and the resistive component could be 1000Ω or higher. If driving a transmission line, such as a twisted pair, using matching resistors will be sufficient to isolate any subsequent capacitance.

POWER DISSIPATION

The LMP8350 is optimized for maximum performance in the small form factor of the standard SOIC package, and is essentially a dual channel amplifier. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} of 150°C is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMP8350:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}^* (V_S)$, where $V_S = V^+ - V^-$. (Be sure to include any current through the feedback network if V_{OCM} is not mid rail.)
2. Calculate the RMS power dissipated in each of the output stages: P_D (rms) = rms $((V_S - V^+_{OUT}) * I^+_{OUT})$ + rms $((V_S - V^-_{OUT}) * I^-_{OUT})$, where V_{OUT} and I_{OUT} are the voltage and the current measured at the output pins of the differential amplifier as if they were single ended amplifiers and V_S is the total supply voltage.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMP8350 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° - T_{AMB})/ \theta_{JA}$, where T_{AMB} = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SOIC package θ_{JA} is 150°C/W.

NOTE: If V_{OCM} is not 0V then there will be quiescent current flowing in the feedback network. This current should be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

ESD PROTECTION

The LMP8350 is protected against electrostatic discharge (ESD) on all pins. The LMP8350 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMP8350 is driven by a large signal while the device is powered down the ESD diodes will conduct . The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

BOARD LAYOUT

While the main signal path frequencies may be fairly low, the ultra-low distortion and settling time specifications rely on wide internal bandwidths. Precautions usually taken for high speed amplifiers should be followed to maintain the best settling times and lowest distortion specifications. In order to get maximum benefit from the differential circuit architecture, board layout and component selection is very critical. The circuit board should have low a inductance ground plane and well bypassed broad supply lines. External components should be leadless surface mount types. The feedback network and output matching resistors should be composed of short traces and precision resistors (0.1%). The output matching resistors should be placed within 3-4 mm of the amplifier as should the supply bypass capacitors.

The LMP8350 is sensitive to parasitic capacitances on the outputs. Ground and power plane metal should be removed from beneath the amplifier and from beneath R_F and R_G.

With any differential signal path symmetry is very important. Even small amounts of asymmetry will contribute to distortion and balance errors. Special attention should be paid to where the bypass capacitors are grounded, as this also affects settling and distortion performance.

The LMH730154 evaluation board is an example of good layout techniques. Evaluation boards are available for purchase through the product folder on National's web site.

EVALUATION BOARD

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMP8350MA	SOIC	LMH730154

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMP8350MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMP8350MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

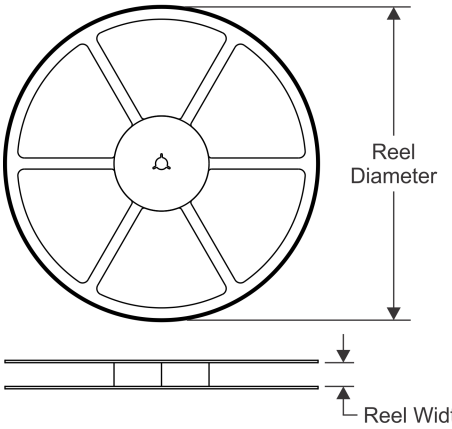
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

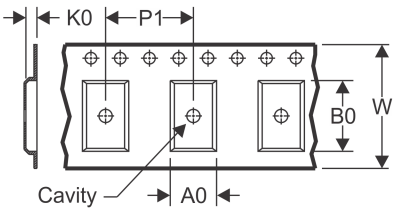
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

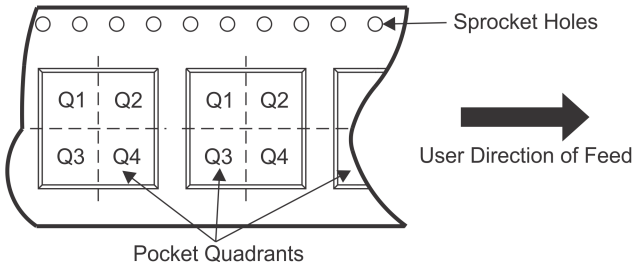


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

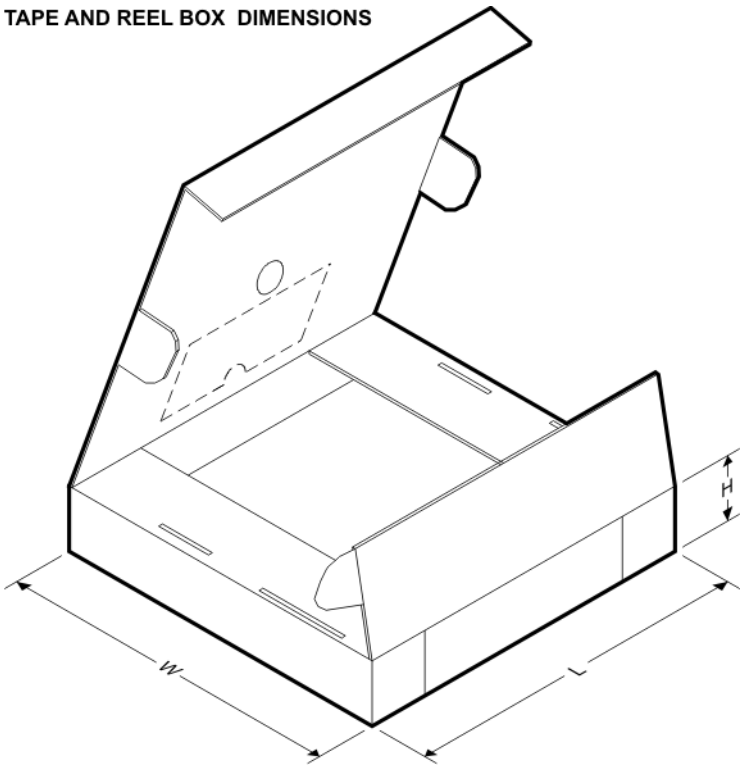
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8350MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

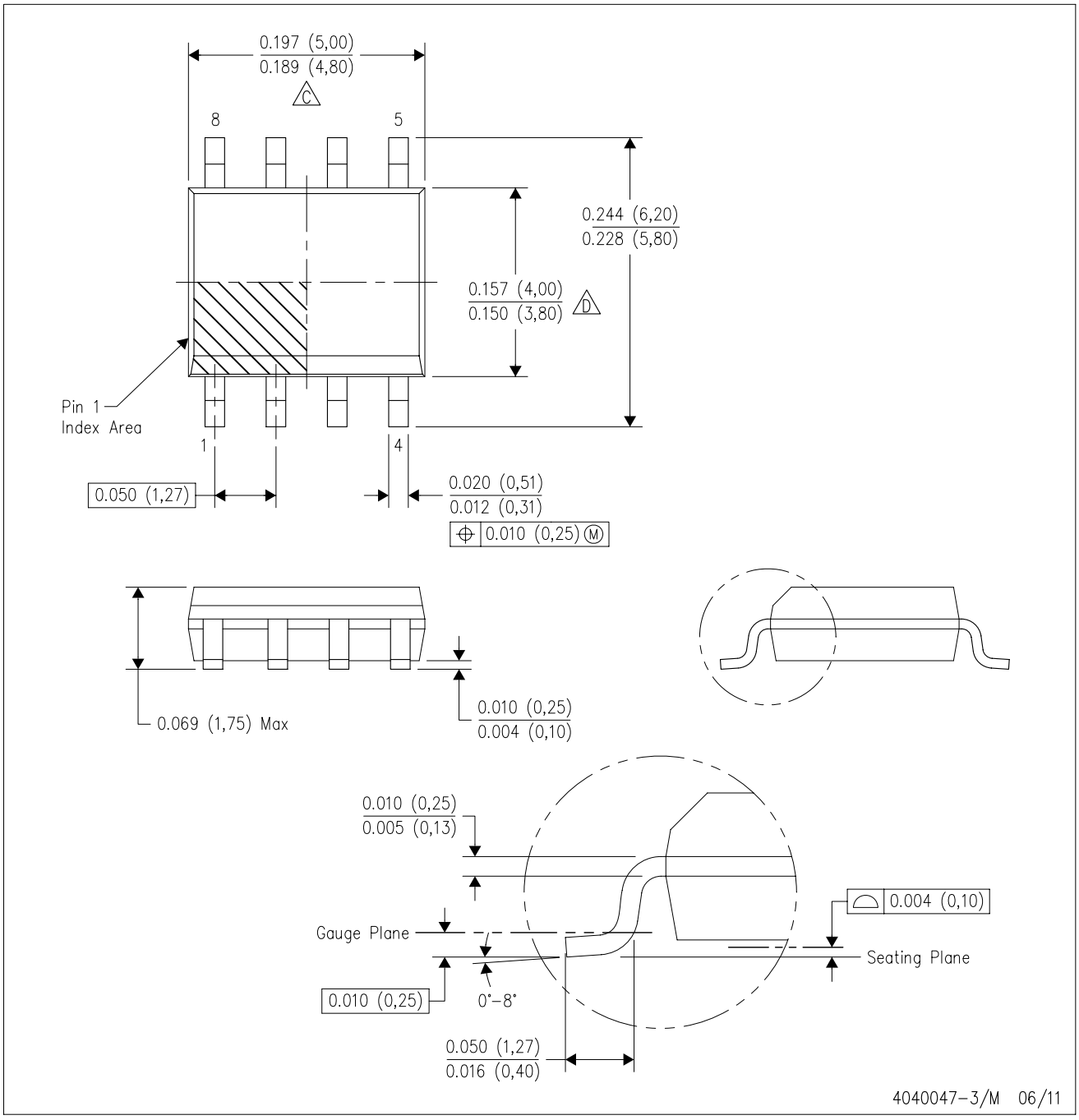
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8350MAX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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