

# DECADE COUNTER | S5490 N7490

S5490-A,F,W • N7490-A,F

DIGITAL 54/74 TTL SERIES

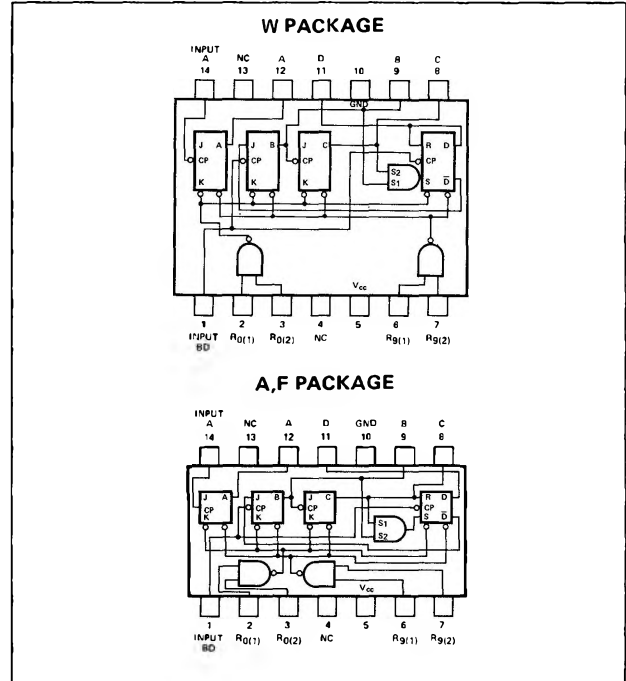
## DESCRIPTION

The S5490/N7490 is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical "0" or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional "0" reset, inputs are provided to reset a BCD 9 count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
3. For operation as a divide-by-two counter and divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

The 5490/7490 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 160mW.

## PIN CONFIGURATIONS



## LOGIC TRUTH TABLES

BCD COUNT SEQUENCE (See Note 1)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	0
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

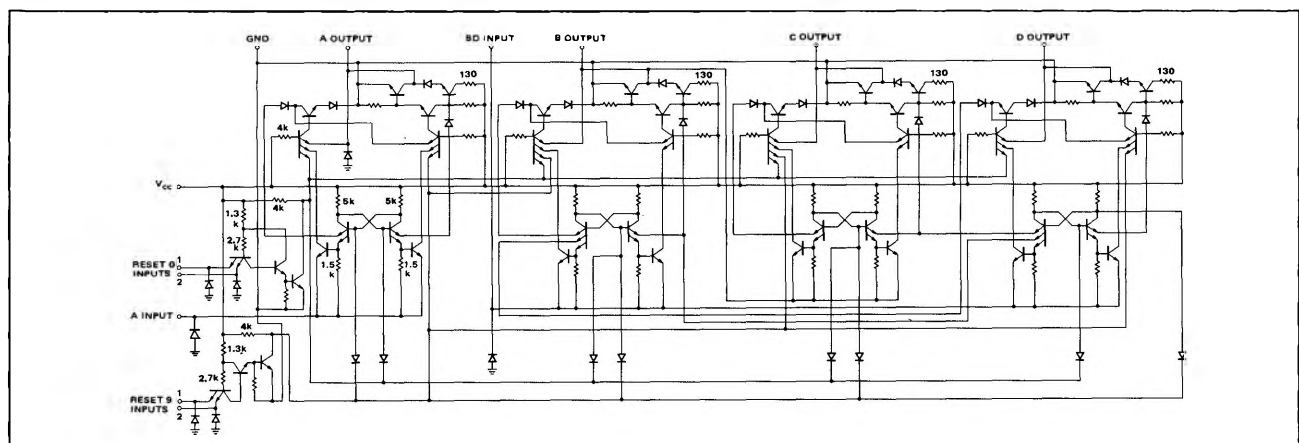
RESET/COUNT (See Note 2)

RESET INPUTS				OUTPUT			
R0(2)	R0(1)	R9(1)	R9(2)	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

### NOTES:

1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.
3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted.

## SCHEMATIC DIAGRAM



**SIGNETICS DIGITAL 54/74 TTL SERIES - S5490 • N7490**

**RECOMMENDED OPERATING CONDITIONS**

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S5490 Circuits	4.5	5	5.5	V
N7490 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns
Operating Free-Air Temperature Range, $T_A$ : S5490 Circuits	-55	25	125	°C
N7490 Circuits	0	25	70	°C

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal $V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal $V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$	Logical 1 output voltage $V_{CC} = \text{MIN}$ , $I_{load} = -400\mu\text{A}$	2.4			V
$V_{out(0)}$	Logical 0 output voltage $V_{CC} = \text{MIN}$ , $I_{sink} = 16\text{mA}$			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{O(1)}$ , $R_{O(2)}$ , $R_{g(1)}$ , or $R_{g(2)}$ $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$			40 1	$\mu\text{A}$ mA
$I_{in(1)}$	Logical 1 level input current at input A $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$			80 1	$\mu\text{A}$ mA
$I_{in(1)}$	Logical 1 level input current at input BD $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$ , $V_{in} = 5.5\text{V}$			160 1	$\mu\text{A}$ mA
$I_{in(0)}$	Logical 0 level input current at $R_{O(1)}$ , $R_{O(2)}$ , $R_{g(1)}$ , or $R_{g(2)}$ $V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A $V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD $V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-6.4	mA
$I_{OS}$	Short circuit output current † $V_{CC} = \text{MAX}$ , $V_{out} = 0\text{V}$			-20 -18	mA mA
$I_{CC}$	Supply current $V_{CC} = \text{MAX}$ , $V_{in} = 4.5\text{V}$			S5490 N7490 32 32	46 53 mA mA

**SWITCHING CHARACTERISTICS,  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ , N = 10**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$	Maximum frequency of input count pulses $C_L = 15\text{pF}$ , $R_L = 400\Omega$	10	18		MHz
$t_{pd1}$	Propagation delay time to logical 1 level from input count pulse to output C $C_L = 15\text{pF}$ , $R_L = 400\Omega$		60	100	ns
$t_{pd0}$	Propagation delay time to logical 0 level from input count pulse to output C $C_L = 15\text{pF}$ , $R_L = 400\Omega$		60	100	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

\*\* All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

† Not more than one output should be shorted at a time.