signetics

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

S54S153
N74S153

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monolithic Schottky-barrier-diode-clamped TTL circuits are high-performance multiplexers which are significantly faster than the S54153/N74153. As an example, the two-gate-level delay from the data inputs to the output is only 8.5 nanoseconds maximum compared to 18 or 23 nanoseconds maximum for the standard-speed part. Overall, the guaranteed delay times for the S54S153/N74S153 represent approximately a 100% improvement over standard TTL with only a 12% increase in maximum d-c power consumption. In many cases, the S54S153 or N74S153 can plug into existing systems designed for S54153 or N74153.

These data selectors/multiplexers are fully compatible for use with most standard, high-speed, and low-power TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54S/74S load, and full fan-out to 10 normalized Series 54S/74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normalized Series 54S/74S loads is provided at high logic levels to facilitate connection of unused inputs to used inputs. Typical power dissipation is 225 milliwatts.

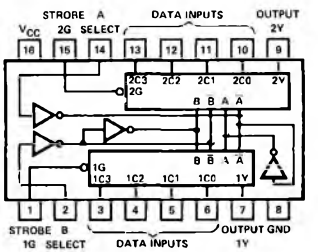
The S54S153 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74S153 is characterized for operation from 0°C to 70°C.

FEATURES

- FULL SCHOTTKY-BARRIER-DIODE CLAMPING FOR VERY HIGH SPEEDS
- PERMITS MULTIPLEXING FROM N LINES TO 1 LINE
- SAME PIN ASSIGNMENTS AS S54153 AND N74153
- STROBE (ENABLE) LINE PROVIDED FOR CASCADING (N LINES TO n LINES)
- TYPICAL AVERAGE PROPAGATION DELAY TIMES:
  - DATA INPUT TO OUTPUT (2 GATE LEVELS) 6 ns
  - STROBE INPUT TO OUPUT (3 GATE LEVELS) 9.5 ns
  - SELECT INPUT TO OUTPUT (4 GATE LEVELS) 12 ns
- HIGH FAN-OUT LOW-IMPEDANCE TOTEM-POLE OUTPUTS
- FULLY COMPATIBLE WITH MOST TTL AND DTL CIRCUITS

PIN CONFIGURATION

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



LOGIC: SEE FUNCTION TABLE

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = High level, L = Low level, X = Irrelevant

RECOMMENDED OPERATING CONDITIONS

		S54S153			N74S153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,		Series 54S	2.5	3.4		V
		V_{IL} = 0.8 V,	I_{OH} = −1 mA	Series 74S	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX			−40		−100	mA
I_{CCL}	Supply current, low level output	V_{CC} = MAX,	See Note 1			45	70	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.
NOTE: 1: I_{CCL} is measured with the outputs open and all inputs grounded.

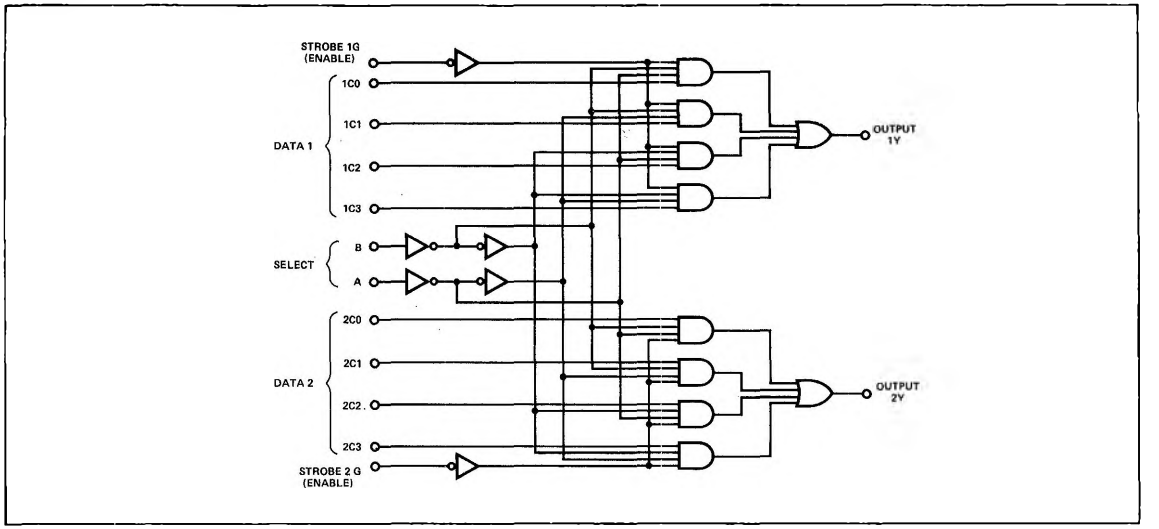
SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 280 Ω, See Note 2		6	9	ns
t_{PHL}	Data	Y			6	9	ns
t_{PLH}	Select	Y			11.5	18	ns
t_{PHL}	Select	Y			12	18	ns
t_{PLH}	Strobe	Y			10	15	ns
t_{PHL}	Strobe	Y			9	13.5	ns

t_{PLH} = Propagation delay time, low-to-high-level output.
t_{PHL} = Propagation delay time, high-to-low-level output.

NOTE 2: Load circuit and test waveforms are shown on page 2-293

FUNCTIONAL BLOCK DIAGRAM



TEST TABLE FOR NOTE 2

INPUTS							OUTPUT Y WAVEFORM
B	A	C0	C1	C2	C3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5 V	X	INPUT	X	X	GND	A
4.5 V	GND	X	X	INPUT	X	GND	A
4.5 V	4.5 V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5 V	X	X	GND	A
INPUT	GND	GND	X	4.5 V	X	GND	A
GND	GND	4.5 V	X	X	X	INPUT	B

X = Irrelevant A=IN-PHASE OUTPUT
B=OUT-OF-PHASE