NCP4304A, NCP4304B

Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies

The NCP4304A/B is a full featured controller and driver tailored to control synchronous rectification circuitry in switch mode power supplies. Due to its versatility, it can be used in various topologies such as flyback, forward and Half Bridge Resonant LLC.

The combination of externally adjustable minimum on and off times helps to fight the ringing induced by the PCB layout and other parasitic elements. Therefore, a reliable and noise less operation of the SR system is insured.

The extremely low turn off delay time, high sink current capability of the driver and automatic package parasitic inductance compensation system allow to maximize synchronous rectification MOSFET conduction time that enables further increase of SMPS efficiency.

Finally, a wide operating V_{CC} range combined with two versions of driver voltage clamp eases implementation of the SR system in 24 V output applications.

Features

- Self-Contained Control of Synchronous Rectifier in CCM, DCM, and QR Flyback Applications
- Precise True Secondary Zero Current Detection with Adjustable Threshold
- Automatic Parasitic Inductance Compensation Input
- Typically 40 ns Turn off Delay from Current Sense Input to Driver
- Zero Current Detection Pin Capability up to 200 V
- Optional Ultrafast Trigger Interface for Further Improved Performance in Applications that Work in Deep CCM
- Disable Input to Enter Standby or Low Consumption Mode
- Adjustable Minimum On Time Independent of V_{CC} Level
- Adjustable Minimum Off Time Independent of V_{CC} Level
- 5 A/2.5 A Peak Current Sink/Source Drive Capability
- Operating Voltage Range up to 30 V
- Gate Drive Clamp of Either 12 V (NCP4304A) or 6 V (NCP4304B)
- Low Startup and Standby Current Consumption
- Maximum Frequency of Operation up to 500 kHz
- SOIC−8 Package
- These are Pb-Free Devices

Typical Applications

- Notebook Adapters
- High Power Density AC/DC Power Supplies
- Gaming Consoles
- All SMPS with High Efficiency Requirements

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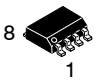
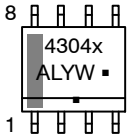
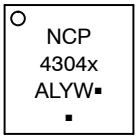
MARKING DIAGRAM



SOIC−8
D SUFFIX
CASE 751



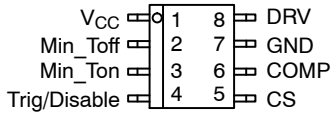
DFN8
CASE 488AF



4304x	= Specific Device Code x = A or B
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(*Note: Microdot may be in either location)

PINOUT INFORMATION



(NOTE: For DFN the exposed pad must be either unconnected or preferably connected to ground. The GND pin must be always connected to ground.)

ORDERING INFORMATION

Device	Package	Shipping†
NCP4304ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP4304BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP4304AMNTWG	DFN8 (Pb−Free)	4000 / Tape & Reel
NCP4304BMNTWG	DFN8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

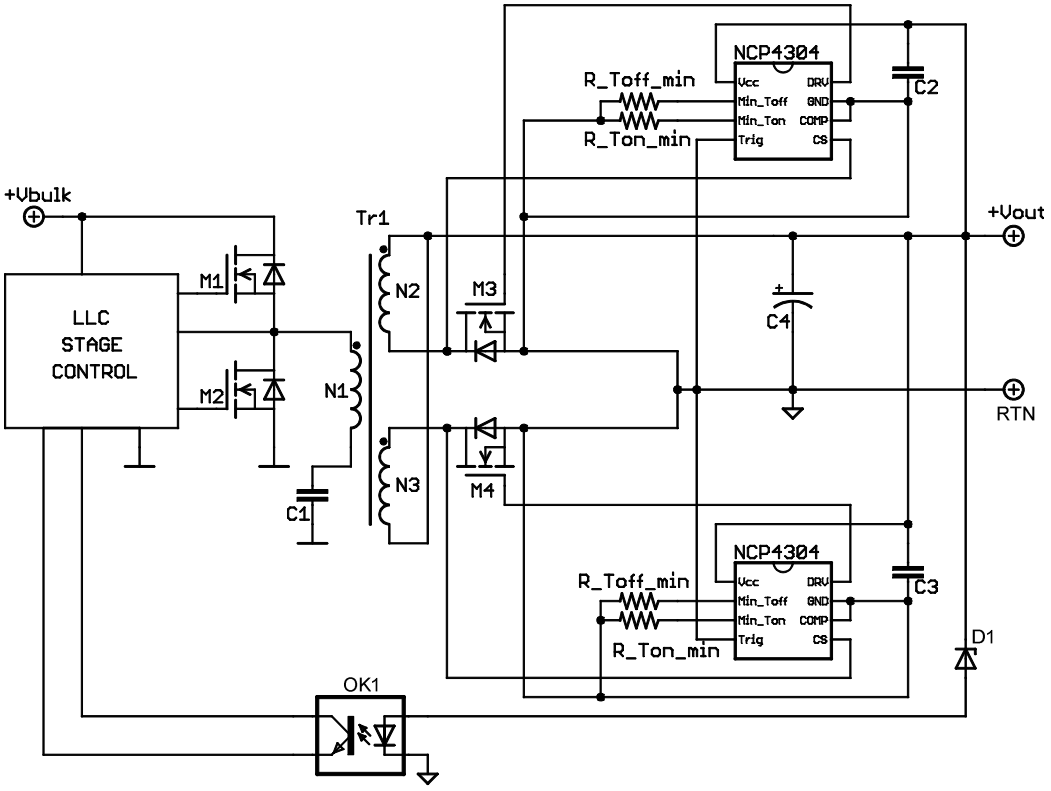


Figure 1. Typical Application Example – LLC Converter

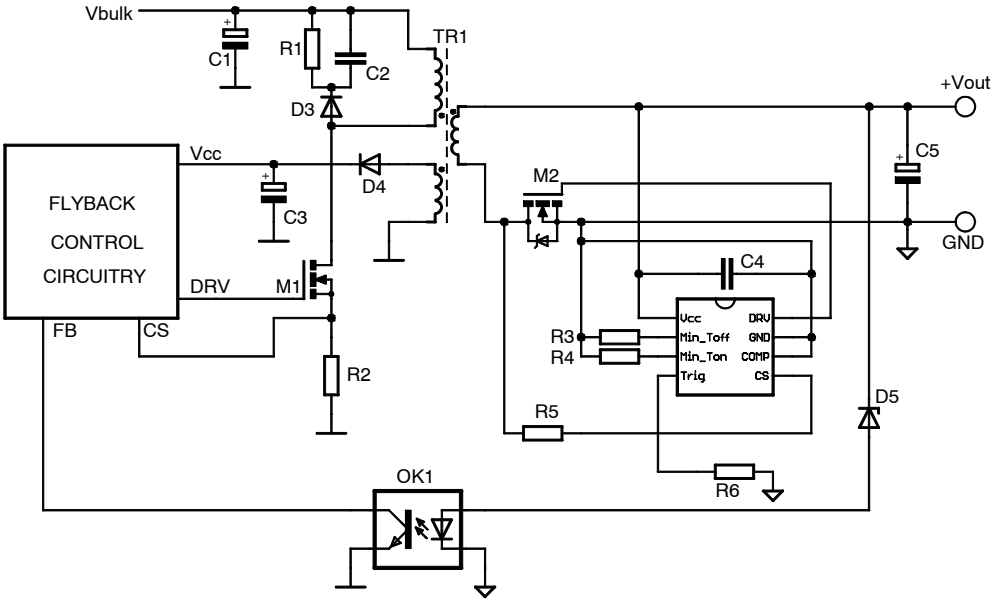


Figure 2. Typical Application Example – DCM or QR Flyback Converter

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	V_{CC}	Supplies the driver	V_{CC} supply terminal of the controller. Accepts up to 30 V continuously.
2	Min_toff	Minimum off time adjust	Adjust the minimum off time period by connecting resistor to ground.
3	Min_ton	Minimum on time adjust	Adjust the minimum on time period by connecting resistor to ground.
4	TRIG/Disable	Forced reset input	This ultrafast input turns off the SR MOSFET in CCM applications. Activates sleep mode if pulled up for more than 100 μs.
5	CS	Current sense of the SR MOSFET	This pin detects if the current flows through the SR MOSFET and/or its body diode. Basic turn off detection threshold is 0 mV. A resistor in series with this pin can modify the turn off threshold if needed.
6	COMP	Compensation inductance connection	Use as a Kelvin connection to auxiliary compensation inductance. If SR MOSFET package parasitic inductance compensation is not used (like for SMT MOSFETs), connect this pin directly to GND pin.
7	GND	IC ground	Ground connection for the SR MOSFET driver and V_{CC} decoupling capacitor. Ground connection for minimum ton, toff adjust resistors and trigger input. GND pin should be wired directly to the SR MOSFET source terminal/soldering point using Kelvin connection.
8	DRV	Gate driver output	Driver output for the SR MOSFET.

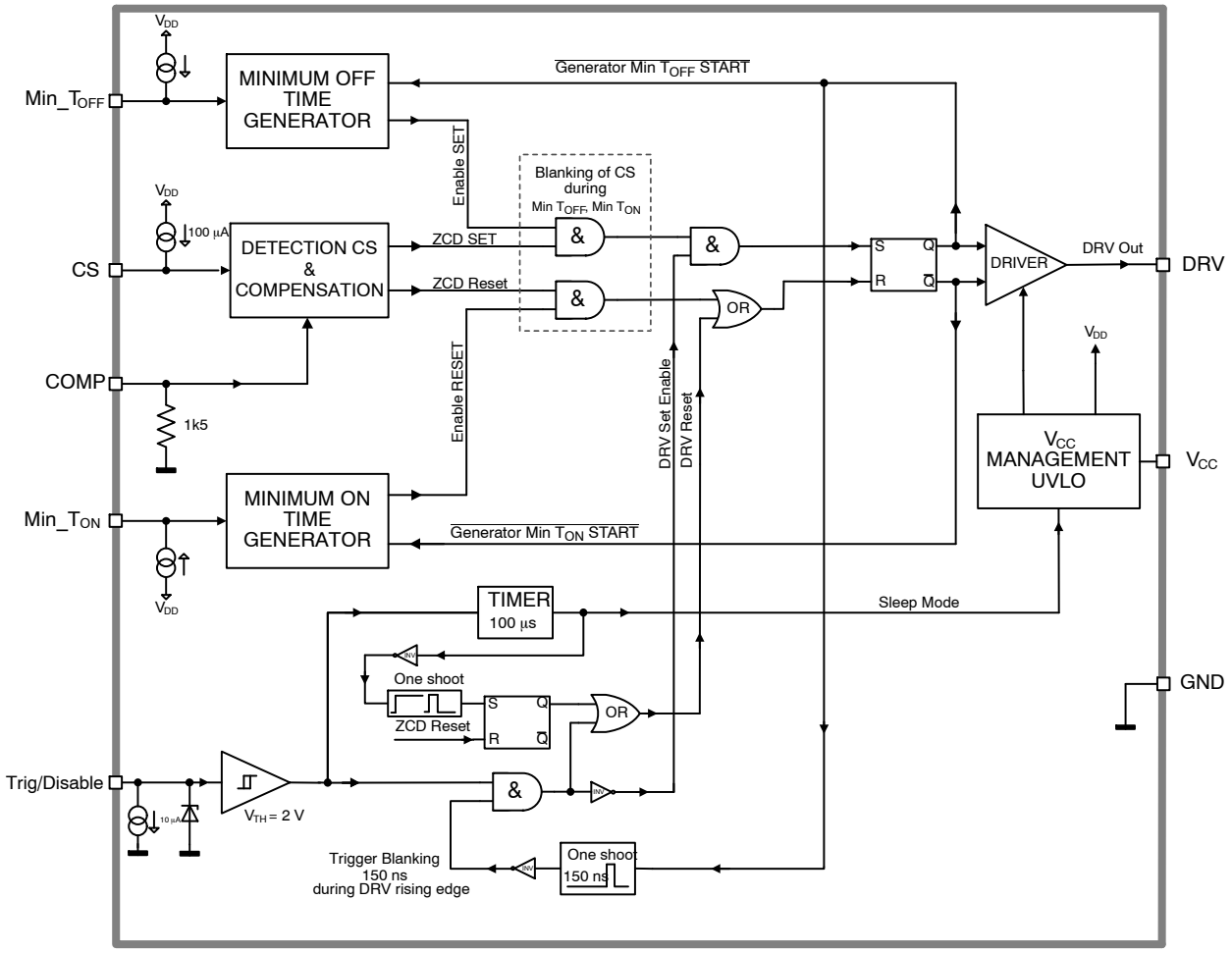


Figure 3. Internal Circuit Architecture

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CC}	IC supply voltage	−0.3 to 30	V
V_{DRV}	Driver output voltage	−0.3 to 17	V
V_{CS}	Current sense input dc voltage	−4 to 200	V
V_{Csdyn}	Current sense input dynamic voltage (t_{pw} = 200 ns)	−10 to 200	V
V_{TRIG}	Trigger input voltage	−0.3 to 10	V
V_{Min_ton}, V_{Min_toff}	Min_Ton and Min_Toff input voltage	−0.3 to 10	V
$I_{\_Min\_Toff}$, $I_{\_Min\_Toff}$	Min_Ton and Min_Toff current	−10 to +10	mA
VGND−COMP	Static voltage difference between GND and COMP pins (internally clamped)	−3 to 10	V
VGND−COMP_dyn	Dynamic voltage difference between GND and COMP pins (t_{pw} = 200 ns)	−10 to 10	V
ICOMP	Current into COMP pin	−5 to 5	mA
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, SOIC − A/B versions	180	°C/W
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, DFN − A/B versions, 50 mm^2 − 1.0 oz. Copper spreader	180	°C/W
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, DFN − A/B versions, 600 mm^2 − 1.0 oz. Copper spreader	80	°C/W
T_{Jmax}	Maximum junction temperature	160	°C
T_{Smax}	Storage Temperature Range	−60 to +150	°C
T_{Lmax}	Lead temperature (Soldering, 10 s)	300	°C
	ESD Capability, Human Body Model except pin V_{CS} − pin 5, HBM ESD Capability on pin 5 is 650 V	2	kV
	ESD Capability, Machine Model	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1−8: Human Body Model 2000 V per JEDEC Standard JESD22−A114E.
   Machine Model Method 200 V pre JEDEC Standard JESD22−A115−A
2. This device meets latchup tests defined by JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V, C_{load} = 0 nF, $R_{\_min\_ton}$ = $R_{\_min\_toff}$ = 10 kΩ, V_{trig} = 0 V, f_CS = 100 kHz, DC_CS = 50%, V_{CS_high} = 4 V, V_{CS_low} = −1 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
V_{CC_on}	Turn−on threshold level (V_{CC} going up)	1	9.3	9.9	10.5	V
V_{CC_off}	Minimum operating voltage after turn−on (V_{CC} going down)	1	8.3	8.9	9.5	V
V_{CC_hyste}	V_{CC} hysteresis	1	0.6	1.0	1.4	V
I_{CC1_A} I_{CC1_B}	Internal IC consumption (no output load on pin 8, F_{sw} = 500 kHz, T_{on_min} = 500 ns, T_{off_min} = 620 ns)	1	− −	4.5 4.0	6.6 6.2	mA
I_{CC2_A} I_{CC2_B}	Internal IC consumption (C_{load} = 1 nF on pin 8, F_{sw} = 400 kHz, T_{on_min} = 500 ns, T_{off_min} = 620 ns)	1	− −	9.0 6.5	12 9	mA
I_{CC3_A} I_{CC3_B}	Internal IC consumption (C_{load} = 10 nF on pin 8, F_{sw} = 400 kHz, T_{on_min} = 500 ns, T_{off_min} = 620 ns)	1	− −	57.0 35.0	80 65	mA
$I_{CC\_StartUp}$	Startup current consumption (V_{CC} = V_{CC_on} − 0.1 V, no switching at CS pin)	1	−	35	75	μA
$I_{CC\_Disable\_1}$	Current consumption during disable mode (No switching at CS pin, V_{trig} = 5 V)	1	−	45	90	μA
$I_{CC\_Disable\_2}$	Current consumption during disable mode (CS pin is switching, F_{sw} = 500 kHz, V_{CS_high} = 4 V, V_{CS_low} =−1 V, V_{trig} = 5 V)	1	−	200	330	μA

3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V, C_{load} = 0 nF, $R_{\_min\_ton}$ = $R_{\_min\_toff}$ = 10 kΩ, V_{trig} = 0 V, f_CS = 100 kHz, DC_CS = 50%, V_{CS_high} = 4 V, V_{CS_low} = −1 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
DRIVE OUTPUT						
t_{r_A}	Output voltage rise−time for A version (C_{load} = 10 nF)	8	–	120	–	ns
t_{r_B}	Output voltage rise−time for B version (C_{load} = 10 nF)	8	–	80	–	ns
t_{f_A}	Output voltage fall−time for A version (C_{load} = 10 nF)	8	–	50	–	ns
t_{f_B}	Output voltage fall−time for B version (C_{load} = 10 nF)	8	–	35	–	ns
R_{oh}	Driver source resistance (Note 3)	8	–	1.8	7	Ω
R_{ol}	Driver sink resistance	8	–	1	2	Ω
$I_{DRV\_pk(source)}$	Output source peak current	8	–	2.5	–	A
$I_{DRV\_pk(sink)}$	Output sink peak current	8	–	5	–	A
$V_{DRV(min\_A)}$	Minimum drive output voltage for A version (V_{CC} = V_{CCoff} + 200 mV)	8	8.3	–	–	V
$V_{DRV(min\_B)}$	Minimum drive output voltage for B version (V_{CC} = V_{CCoff} + 200 mV)	8	4.5	–	–	V
$V_{DRV(CLMP\_A)}$	Driver clamp voltage for A version (12 < V_{CC} < 28, C_{load} = 1 nF)	8	10	12	14.3	V
$V_{DRV(CLMP\_B)}$	Driver clamp voltage for B version (12 < V_{CC} < 28, C_{load} = 1 nF)	8	5	6	8	V
CS INPUT						
T_{pd_on}	The total propagation delay from CS input to DRV output turn on (Vcs goes down from 4 V to −1 V, t_{f_CS} = 5 ns, COMP pin connected to GND)	5, 8	–	60	90	ns
T_{pd_off}	The total propagation delay from CS input to DRV output turn off (Vcs goes up from −1 V to 4 V, t_{r_CS} = 5 ns, COMP pin connected to GND), (Note 3)	5, 8	–	40	55	ns
I_{shift_CS}	Current sense input current source (V_{CS} = 0 V)	5	95	100	105	μA
$V_{th\_cs\_on}$	Current sense pin turn−on input threshold voltage	5, 8	−120	−85	−50	mV
$V_{th\_cs\_off}$	Current sense pin turn−off threshold voltage, COMP pin connected to GND (Note 3)	5, 8	−1	–	0	mV
G_{comp}	Compensation inverter gain	5,6,8		−1		–
$I_{CS\_Leakage}$	Current Sense input leakage current, V_{CS} = 200 Vdc	5	–	–	1	μA
TRIGGER/DISABLE INPUT						
$t_{trig\_pw\_min}$	Minimum trigger pulse width (Note 3)	4	30	–	–	ns
V_{trig}	Trigger input threshold voltage (V_{trig} goes up)	4	1.5	–	2.5	V
t_{p_trig}	Propagation delay from trigger input to the DRV output (V_{trig} goes up from 0 to 5 V, t_{r_trig} = 5 ns)	4	–	13	30	ns
$t_{trig\_light\_load}$	Light load turn off filter duration	4	70	100	130	μs
$t_{trig\_light\_load\_rec.}$	IC operation recovery time when leaving light load disable mode (V_{trig} goes down from 5 to 0 V, t_{f_trig} = 5 ns)	4	–	–	10	us
t_{t_blank}	Blanking time of trigger/dis during DRV rising edge (V_{CS} < $V_{th\_cs\_on}$, single pulse on trigger/dis t_{trig_pw} = 50 ns)	4	–	120	–	ns
I_{trig}	Trigger input pull down current (V_{trig} = 5 V)	4	–	10	–	μA
MINIMUM T_{on} AND T_{off} ADJUST						
T_{on_min}	Minimum T_{on} period ($R_{T\_on\_min}$ = 0 Ω)	3	–	130	–	ns
T_{off_min}	Minimum T_{off} period ($R_{T\_off\_min}$ = 0 Ω)	2	560	600	690	ns
T_{on_min}	Minimum T_{on} period ($R_{T\_on\_min}$ = 10 kΩ)	3	0.9	1.0	1.1	μs
T_{off_min}	Minimum T_{off} period ($R_{T\_off\_min}$ = 10 kΩ)	2	0.9	1.0	1.1	μs
T_{on_min}	Minimum T_{on} period ($R_{T\_on\_min}$ = 50 kΩ)	3	–	4.8	–	μs
T_{off_min}	Minimum T_{off} period ($R_{T\_off\_min}$ = 50 kΩ)	2	–	4.8	–	μs

3. Guaranteed by design.

TYPICAL CHARACTERISTICS

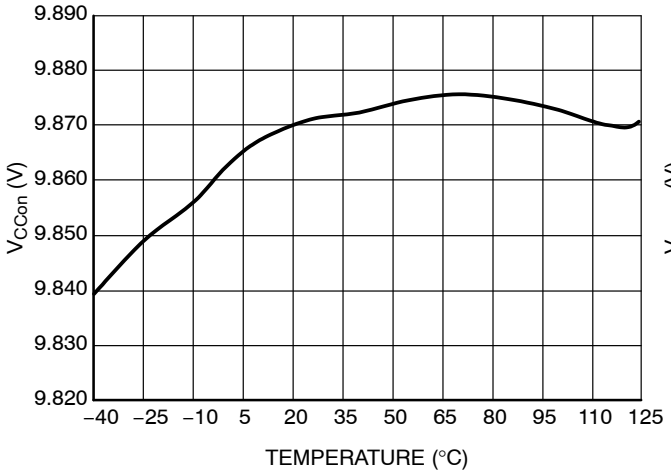


Figure 4. V_{CC} Startup Voltage

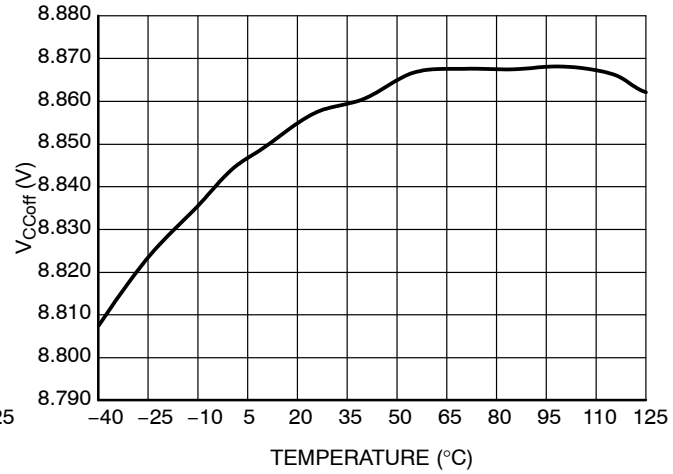


Figure 5. V_{CC} Turn−off Voltage

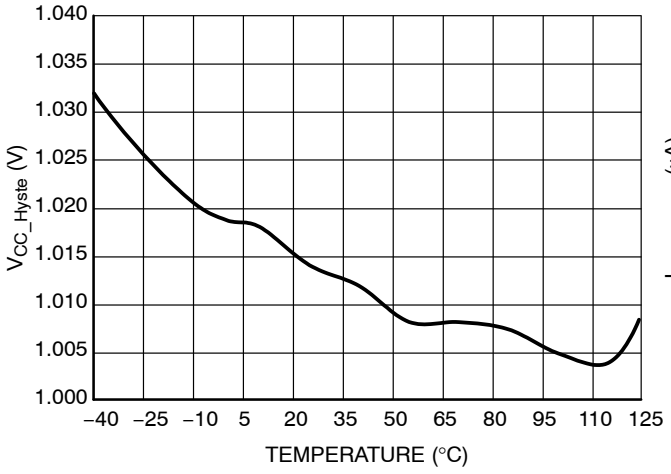


Figure 6. V_{CC} Hysteresis

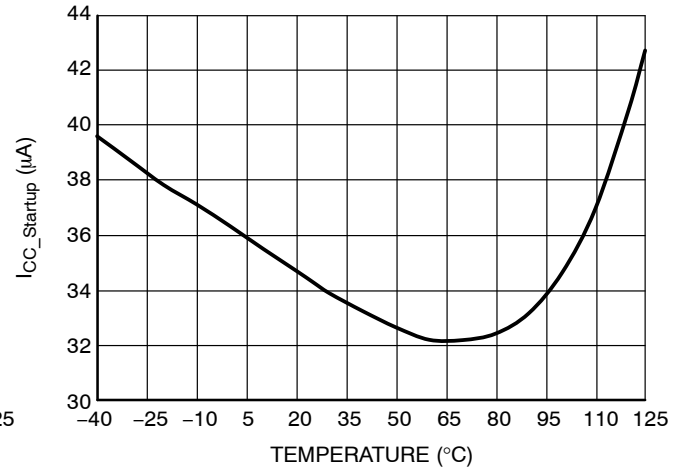


Figure 7. Startup Current

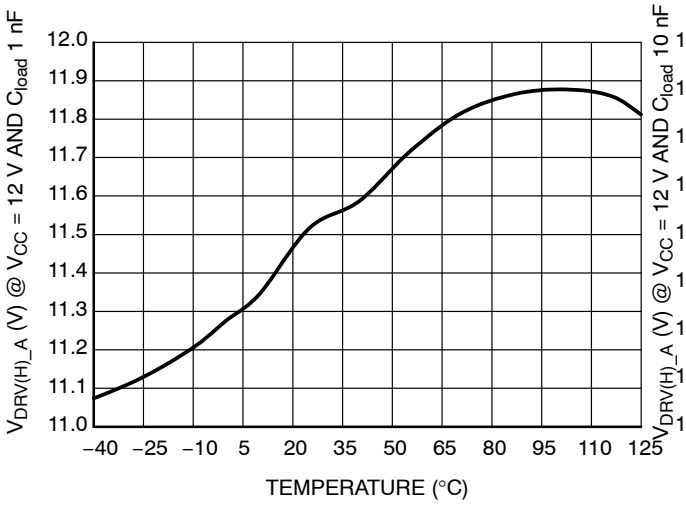


Figure 8. Driver High Level – A Version, V_{CC} = 12 V and C_{load} = 1 nF

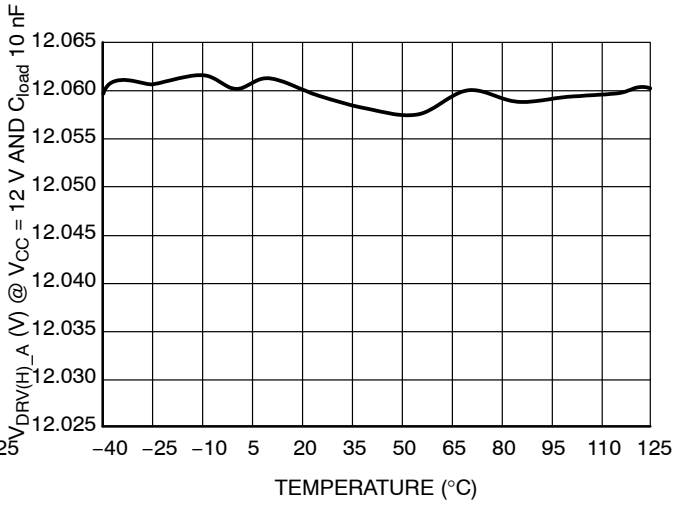


Figure 9. Driver High Level – A Version, V_{CC} = 12 V and C_{load} = 10 nF

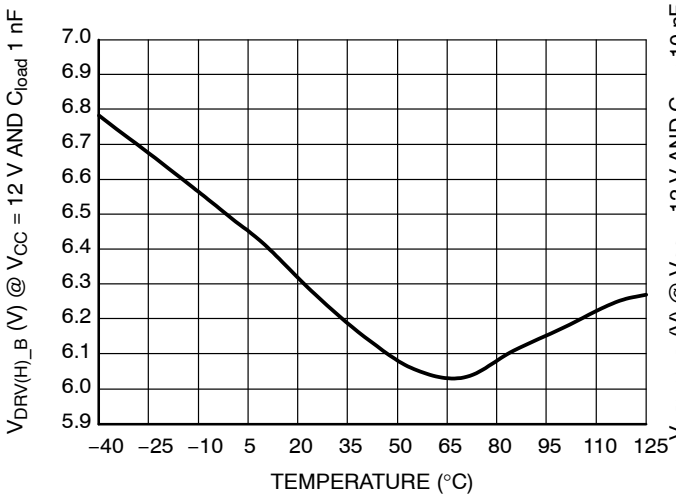


Figure 10. Driver High Level – B Version, V_{CC} = 12 V and C_{load} = 1 nF

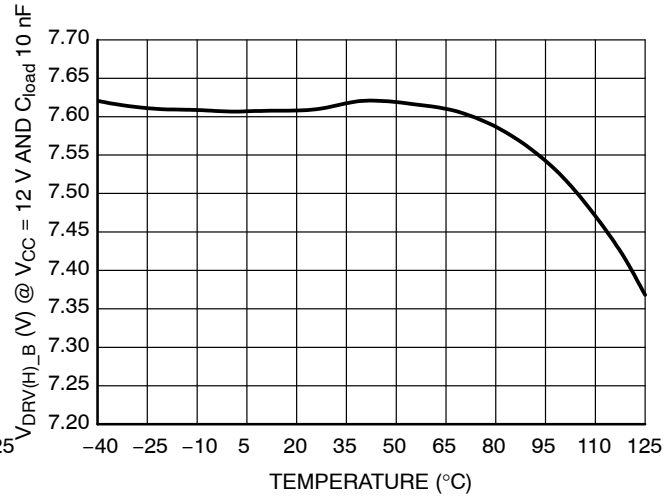


Figure 11. Driver High Level – B Version, V_{CC} = 12 V and C_{load} = 10 nF

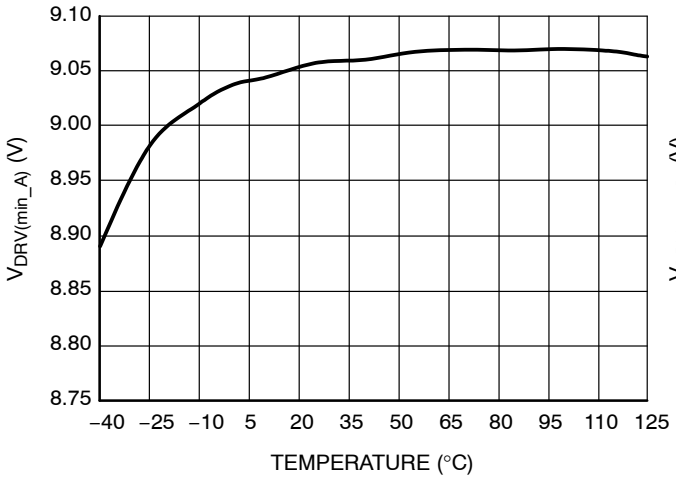


Figure 12. Minimal Driver High Level−A Version, V_{CC_OFF} + 0.2 V and C_{load} = 0 nF

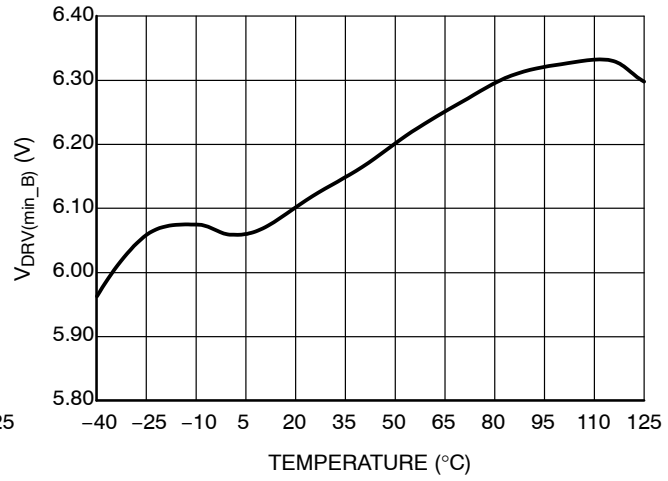


Figure 13. Minimal Driver High Level−B Version, V_{CC_OFF} + 0.2 V and C_{load} = 0 nF

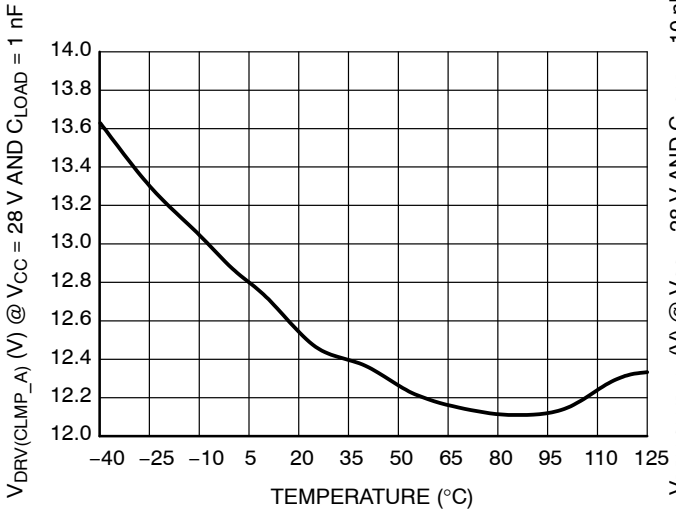


Figure 14. Driver Clamp Level−A Version, V_{CC} = 28 V and C_{load} = 1 nF

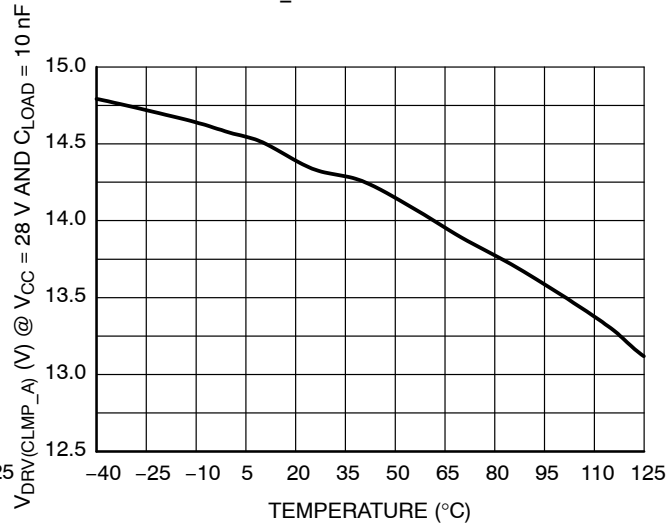


Figure 15. Driver Clamp Level−A Version, V_{CC} = 28 V and C_{load} = 10 nF

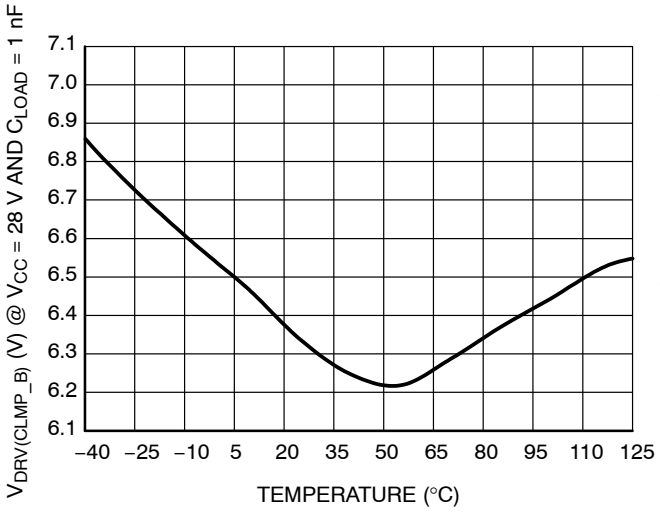


Figure 16. Driver Clamp Level−B Version, V_{CC} = 28 V and C_{load} = 1 nF

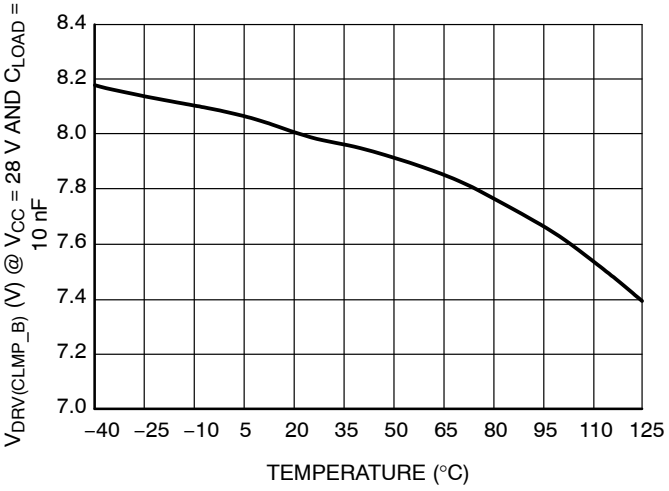


Figure 17. Driver Clamp Level−B Version, V_{CC} = 28 V and C_{load} = 10 nF

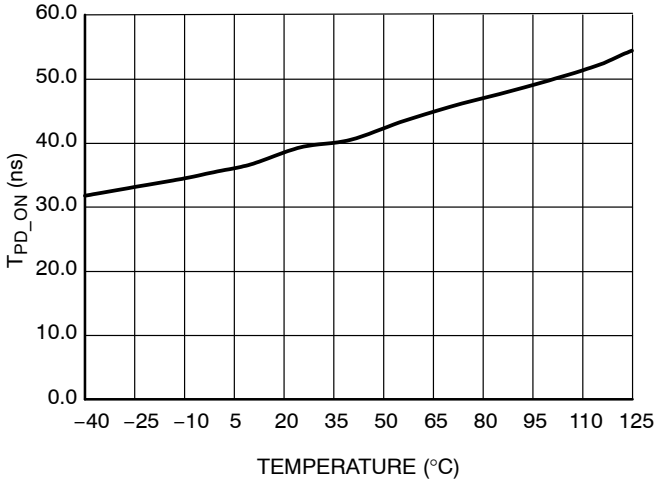


Figure 18. CS to DRV Turn−on Propagation Delay

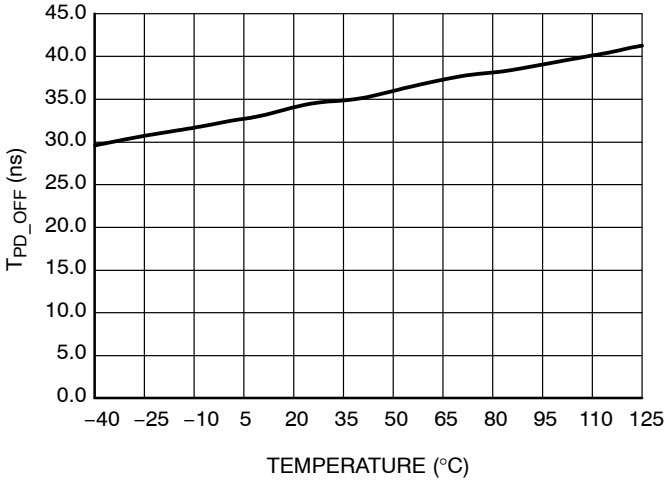


Figure 19. CS to DRV Turn−off Propagation Delay

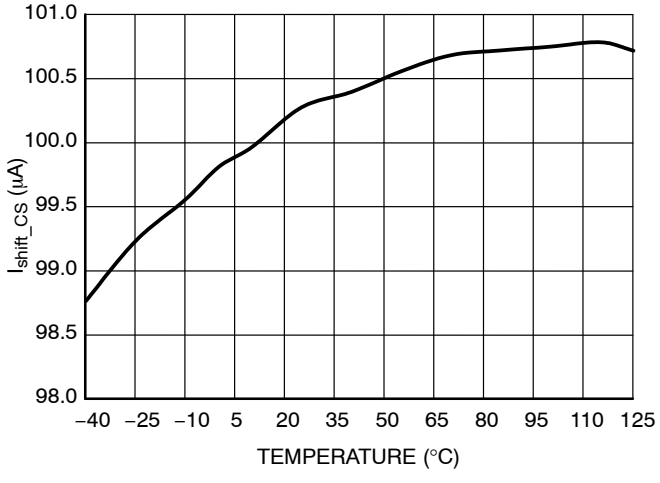


Figure 20. CS Pin Shift Current

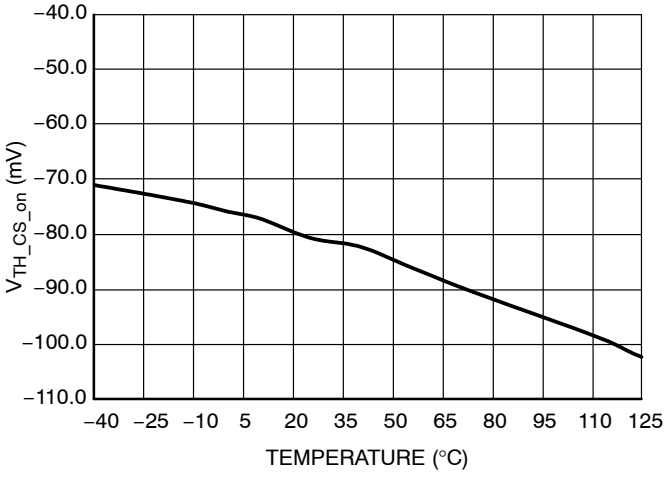


Figure 21. CS Turn−on Threshold

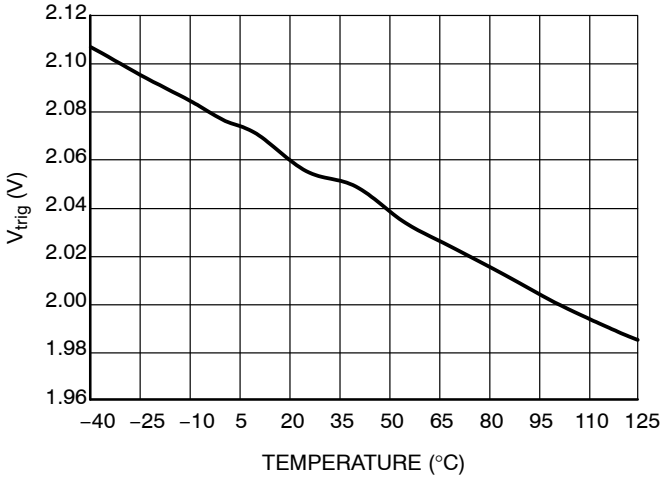


Figure 22. Trigger Input Threshold Voltage

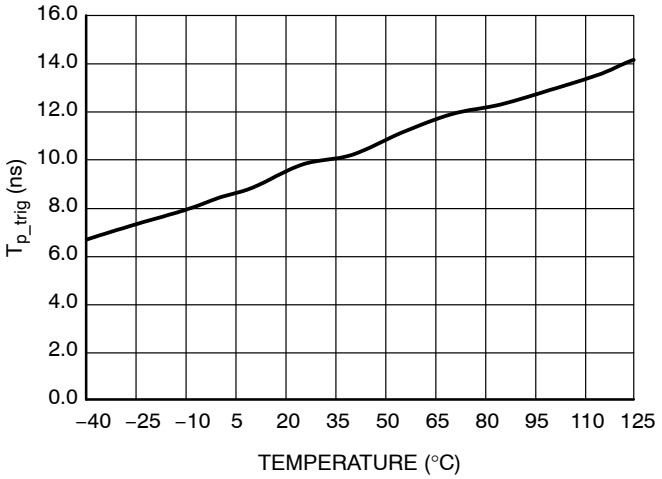


Figure 23. Progagation Delay from Trigger Input to DRV Turn−off

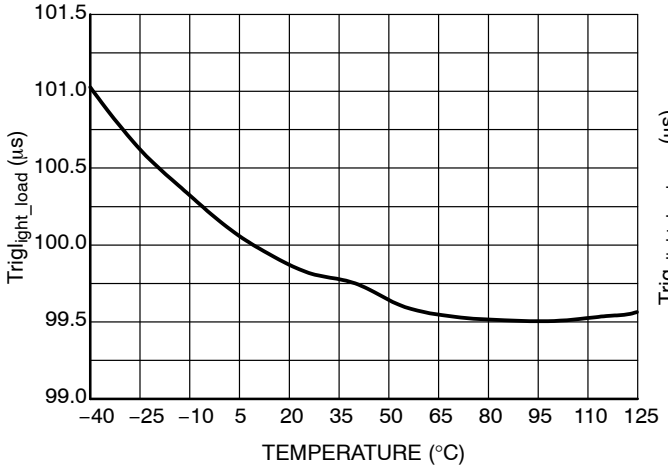


Figure 24. Light Load Transition Timer Duration

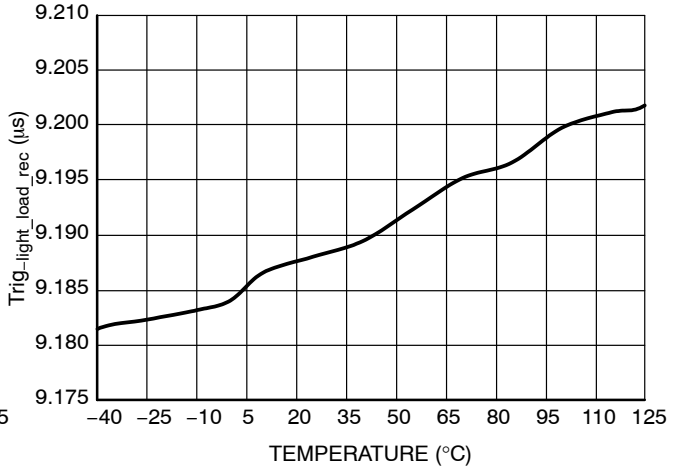


Figure 25. Light Load to Normal Operation Recovery Time

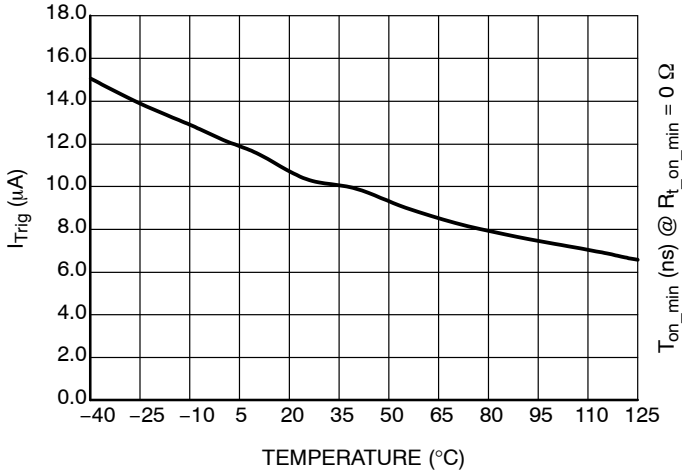


Figure 26. Trigger Input Pulldown Current

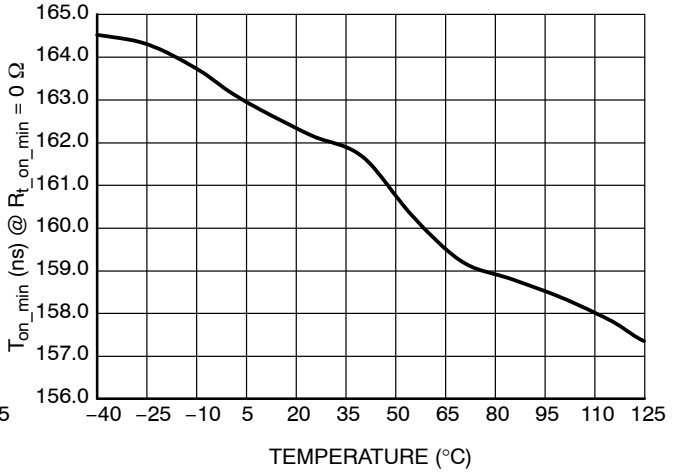


Figure 27. Minimum on Time @ $R_{t\_on\_min}$ = 0 Ω

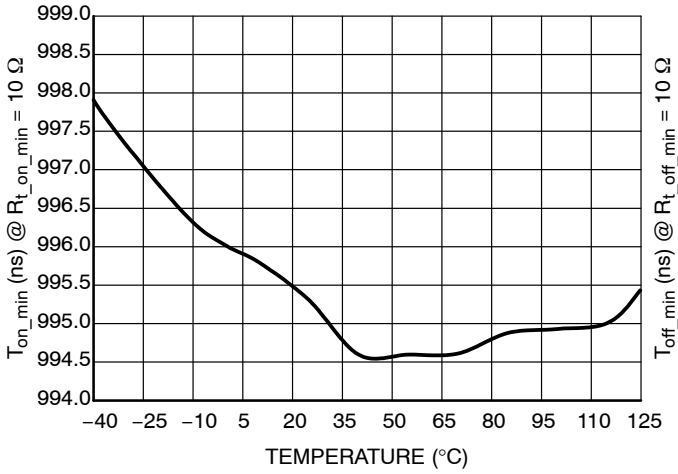


Figure 28. Minimum On Time @ $R_{t\_on\_min}$ = 10 Ω

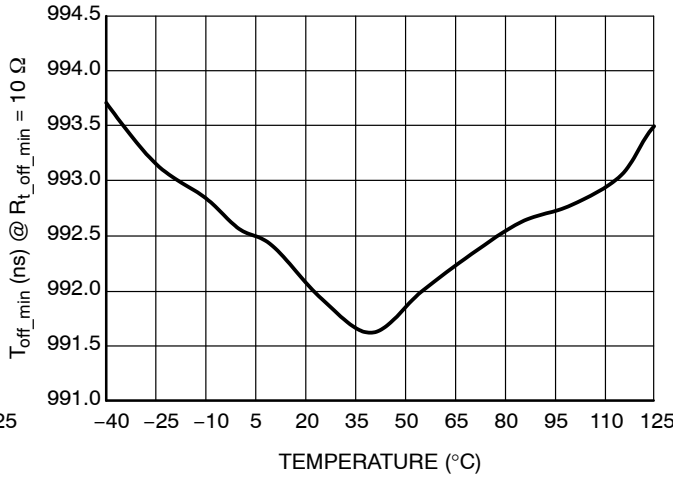


Figure 29. Minimum Off Time @ $R_{t\_off\_min}$ = 10 Ω

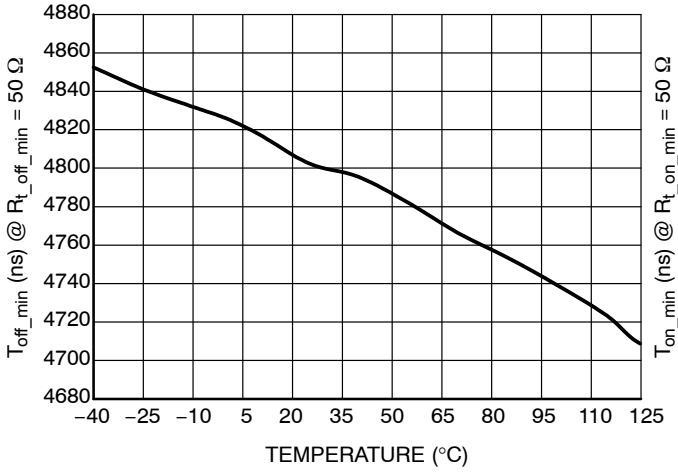


Figure 30. Minimum On Time @ $R_{t\_on\_min}$ = 53 Ω

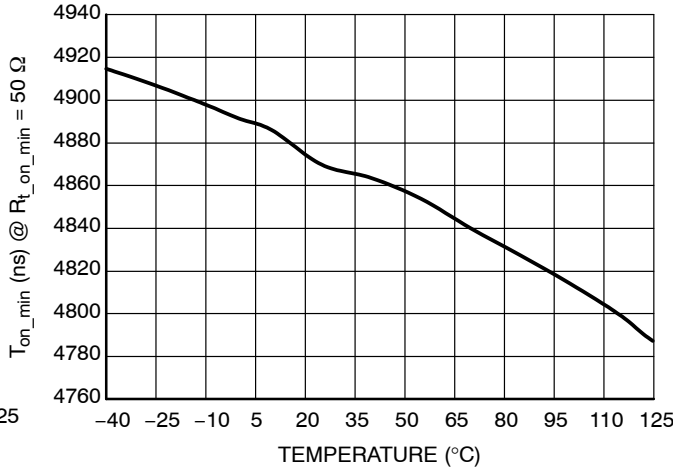


Figure 31. Minimum Off Time @ $R_{t\_off\_min}$ = 53 Ω

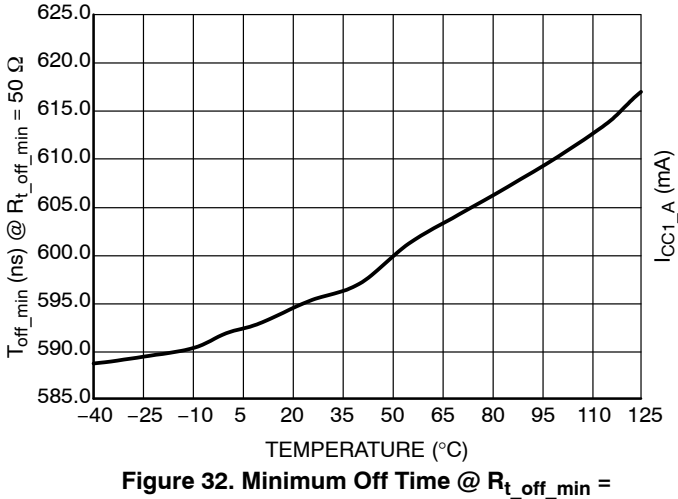


Figure 32. Minimum Off Time @ $R_{t\_off\_min}$ = 0 Ω

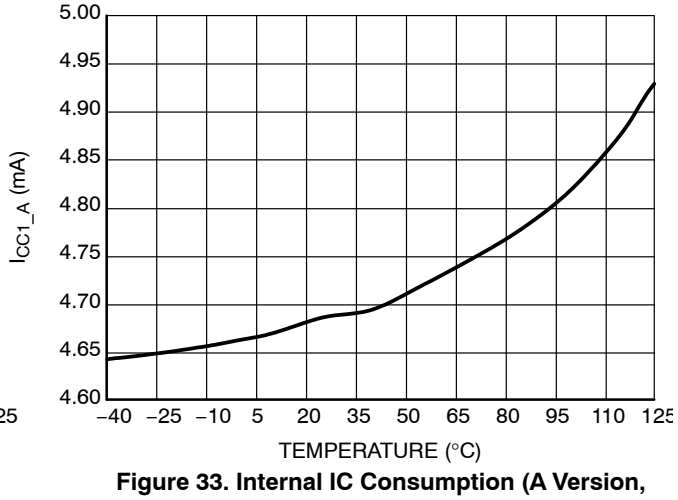


Figure 33. Internal IC Consumption (A Version, No Load on Pin 8, F_{SW} = 500 kHz, T_{on_min} = 500 ns, T_{off_min} = 620 ns)

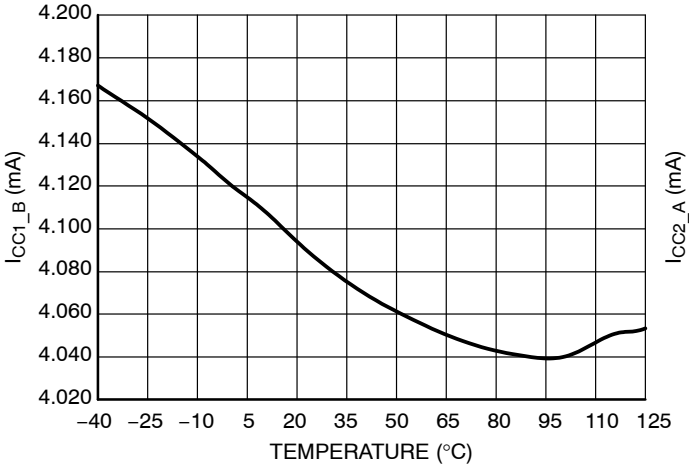


Figure 34. Internal IC Consumption (B version, No Load on Pin 8, F_{SW} = 500 kHz, T_{on_min} = 500 ns, T_{off_min} = 620 ns)

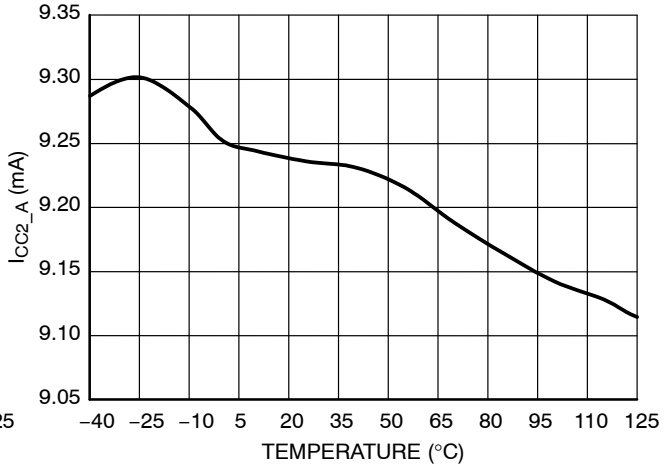


Figure 35. Internal IC Consumption (A Version, C_{load} = 1 nF on Pin 8, F_{SW} = 400 kHz, T_{on_min} = 500 ns, T_{off_min} = 620 ns)

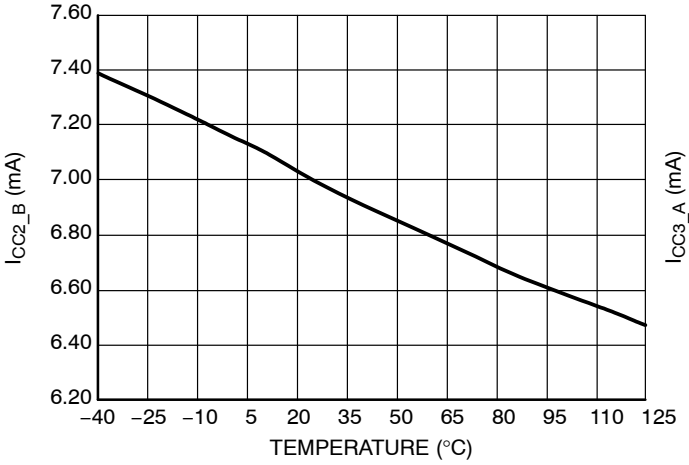


Figure 36. Internal IC Consumption (B Version, C_{load} = 1 nF on Pin 8, F_{SW} = 400 kHz, T_{on_min} = 500 ns, T_{off_min} = 620 ns)

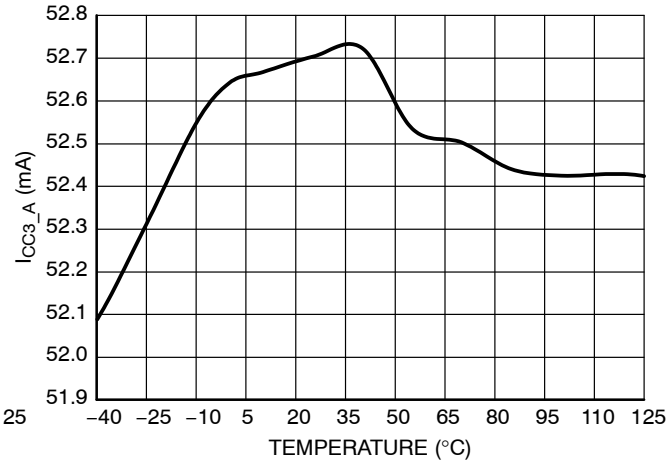


Figure 37. Internal IC Consumption (A Version, C_{load} = 10 nF on Pin 8, F_{SW} = 400 kHz, T_{on_min} = 500 ns, T_{off_min} = 620 ns)

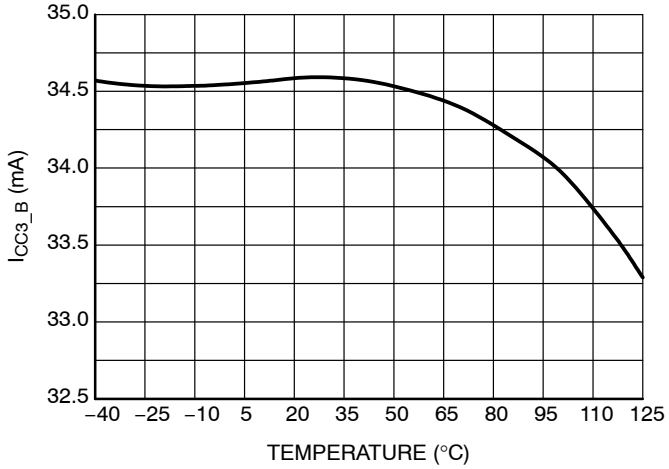


Figure 38. Internal IC Consumption (B Version, C_{load} = 10 nF on Pin 8, F_{SW} = 400 kHz, T_{on_min} = 500 ns, T_{off_min} = 620 ns)

APPLICATION INFORMATION

General Description

The NCP4304A/B is designed to operate either as a standalone IC or as a companion IC to a primary side controller to help achieve efficient synchronous rectification in switch mode power supplies. This controller features a high current gate driver along with high−speed logic circuitry to provide appropriately timed drive signals to a synchronous rectification MOSFET. With its novel architecture, the NCP4304A/B has enough versatility to keep the synchronous rectification efficient under any operating mode.

The NCP4304A/B works from an available bias supply with voltage range from 10.4 V to 28 V (typical). The wide V_{CC} range allows direct connection to the SMPS output voltage of most adapters such as notebook and LCD TV adapters. As a result, the NCP4304A/B simplifies circuit operation compared to other devices that require specific bias power supplies (e.g. 5 V). The high voltage capability of the V_{CC} is also a unique feature designed to allow operation for a broader range of applications.

Precise turn off threshold of the current sense comparator together with accurate offset current source allows the user to adjust for any required turn off current threshold of the SR MOSFET switch using a single resistor. Compared to other SR controllers that provide turn off thresholds in the range of −10 mV to −5 mV, the NCP4304A/B offers a turn off threshold of 0 mV that in combination with a low $R_{DS(on)}$ SR MOSFET significantly reduces the turn off current threshold and improves efficiency.

To overcome issues after turn on and off events, the NCP4304A/B provides adjustable minimum on time and off time blanking periods. Blanking times can be adjusted independently of IC V_{CC} using resistors connected to GND. If needed, blanking periods can be modulated using additional components.

An ultrafast trigger input helps to implement synchronous rectification systems in CCM applications (like CCM flyback or forward). The time delay from trigger input to driver turn off event is 10 ns (typicaly). Additionally, the trigger input can be used to disable the IC and activate a low consumption standby mode. This feature can be used to decrease standby consumption of an SMPS.

Finally, the NCP4304A/B features a special input that can be used to automatically compensate for SR MOSFET parasitic inductance effect. This technique achieves the maximum available on−time and thus optimizes efficiency when a MOSFET in standard package (like TO−220 or TO247) is used. If a SR MOSFET in SMT package with negligible inductance is used, the compensation input is connected to GND pin.

Zero Current Detection and Parasitic Inductance Compensation

Figure 39 shows the internal connection of the ZCD circuitry on the current sense input. The synchronous rectification MOSFET is depicted with it's parasitic inductances to demonstrate operation of the compensation system.

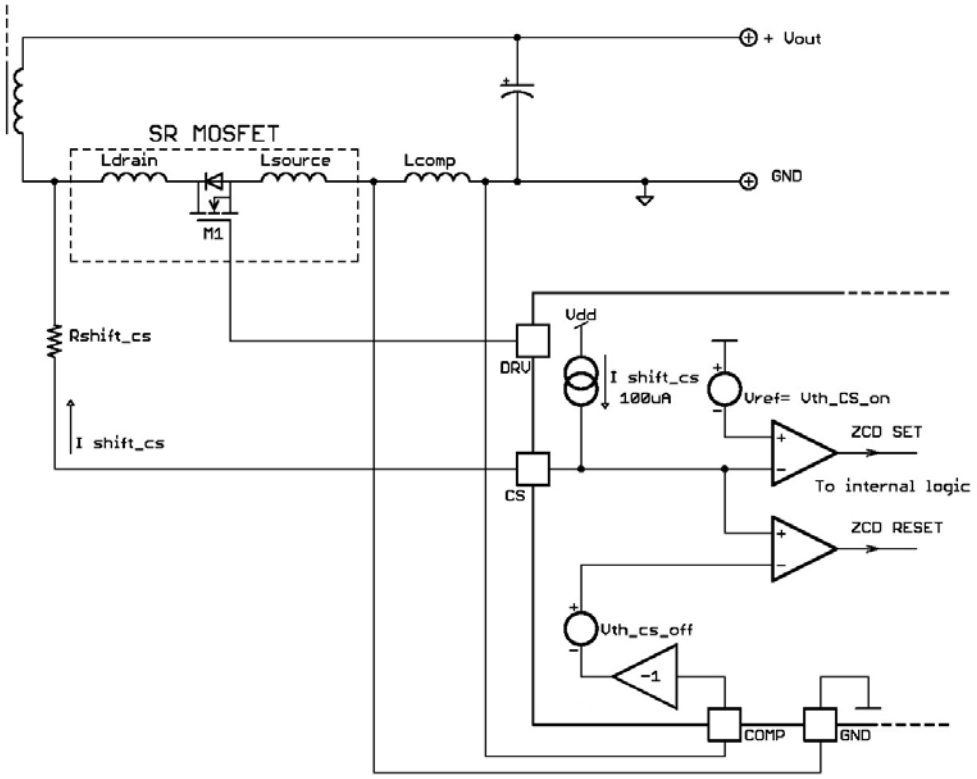


Figure 39. ZCD Sensing Circuitry Functionality

When the voltage on the secondary winding of the SMPS reverses, the body diode of M1 starts to conduct current and the voltage of M1's drain drops approximately to −1 V. The CS pin sources current of 100 μA that creates a voltage drop on the R_{shift_cs} resistor. Once the voltage on the CS pin is lower than $V_{th\_cs\_on}$ threshold, M1 is turned on. Because of parasitic impedances, significant ringing can occur in the application. To overcome sudden turn−off due to mentioned ringing, the minimum conduction time of the SR MOSFET is activated. Minimum conduction time can be adjusted using $R_{\_Min\_Ton}$ resistor.

The SR MOSFET is turned−off as soon as the voltage on the CS pin is higher than $V_{th\_cs\_off}$. For the same ringing reason, a minimum off time timer is asserted once the turn-off is detected. The minimum off time can be externally adjusted using $R_{\_Min\_Toff}$ resistor. MOSFET M1 conducts when the secondary current decreases, therefore the turn−off time depends on its $R_{DS(on)}$. The 0 mV threshold provides an optimum switching period usage while keeping enough time margin for the gate turn off. The R_{shift_cs} resistor provides the designer with the possibility to modify (increase) the actual turn-off current threshold.

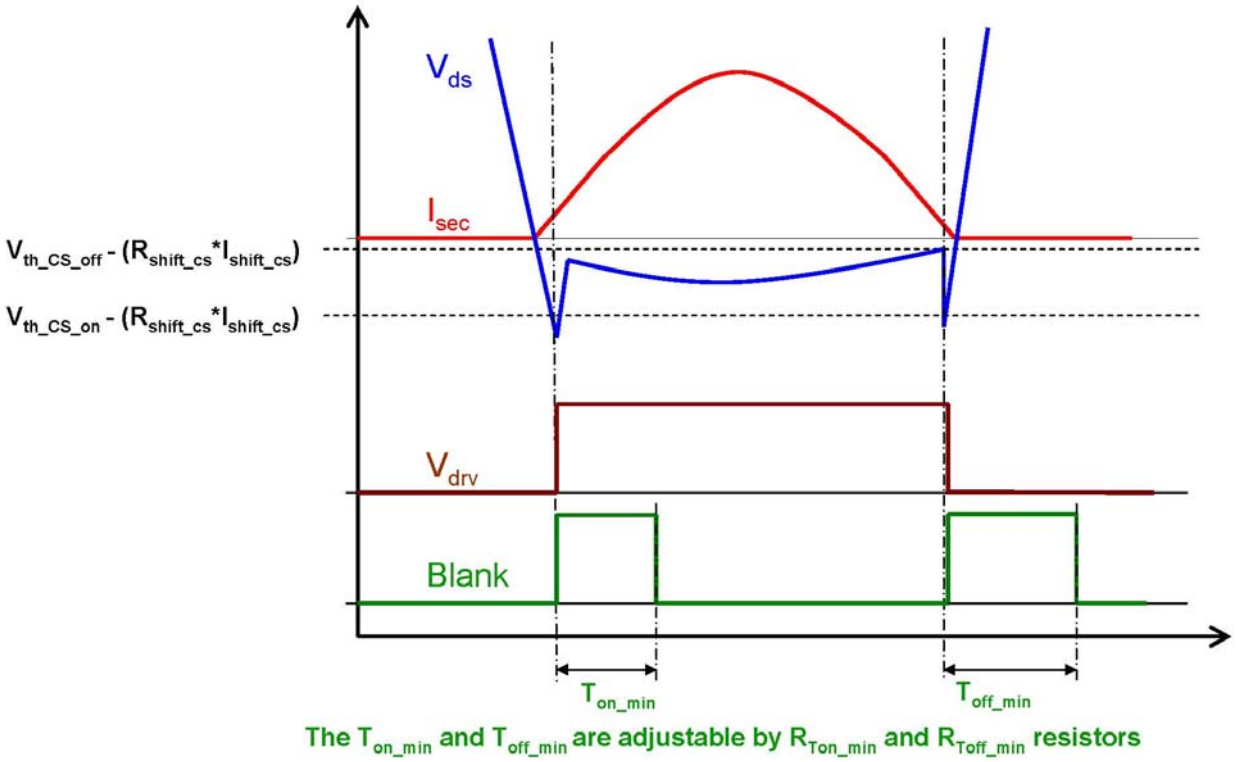


Figure 40. ZCD Comparators Thresholds and Blanking Periods Timing

If no Rshift_cs resistor is used, the turn−on and turn−off thresholds are fully given by the CS input specification (please refer to parametric table). Once non−zero R_{shift_cs} resistor is used, both thresholds move down (i.e. higher MOSFET turn off current) as the CS pin offset current causes a voltage drop that is equal to:

$$V\_Rshift\_cs = Rshift\_cs * Ishift\_cs \quad \text{(eq. 1)}$$

Final turn−on and turn−off thresholds can be then calculated as:

$$VCS\_turn\_on = Vth\_CS\_on - (Rshift\_cs * Ishift\_cs) \quad \text{(eq. 2)}$$

$$VCS\_turn\_off = Vth\_CS\_off - (Rshift\_cs * Ishift\_cs) \quad \text{(eq. 3)}$$

Note that R_{shift_cs} impact on turn−on threshold is less critical compare to turn−off threshold.

If using a SR MOSFET in TO−220 package (or other package which features leads), the parasitic inductance of the package leads causes a turn−off current threshold increase. This is because current that flows through the SR MOSFET has quite high di(t)/dt that induces error voltage on the SR MOSFET leads inductance. This error voltage, that is proportional to the secondary current derivative, shifts the CS input voltage to zero when significant current still flows through the channel. Zero current threshold is thus detected when current still flows through the SR MOSFET channel – please refer to Figure 41 for better understanding. As a result, the SR MOSFET is turned−off prematurely and the efficiency of the SMPS is not optimized.

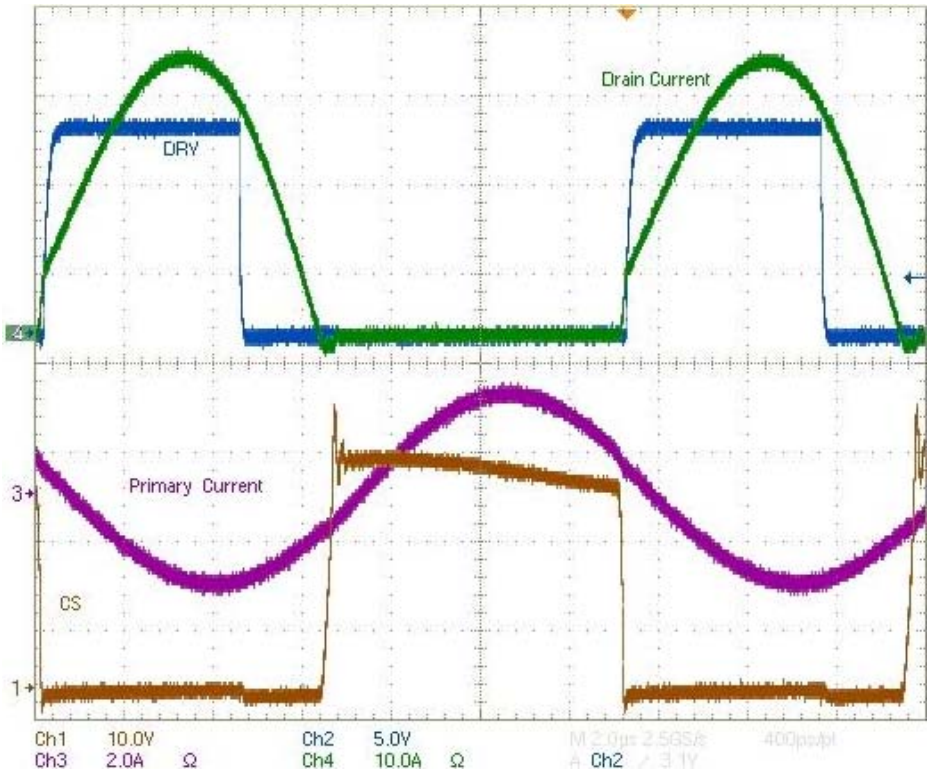


Figure 41. Waveforms from SR System Using MOSFET in TO−220 Package Without Parasitic Inductance Compensation – SR MOSFET Channel Conduction Time is Reduced

Note that the efficiency impact of the error caused by parasitic inductance increases with lower Rds_on MOSFETs and/or higher operating frequency.

The NCP4304A/B offers a way to compensate for MOSFET parasitic inductances effect - refer to Figure 42.

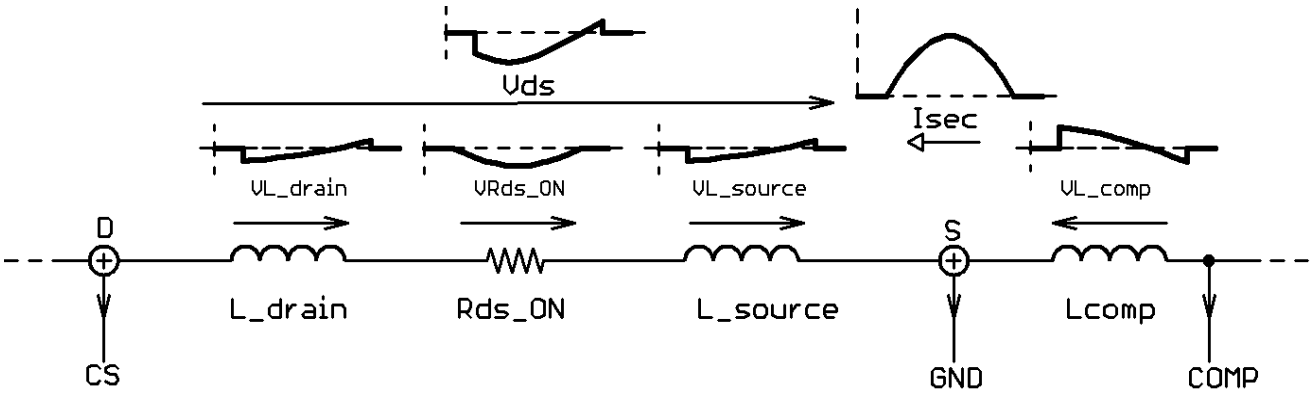


Figure 42. Package Parasitic Inductances Compensation Principle

Dedicated input (COMP) offers the possibility to use an external compensation inductance (wire strap or PCB). If the value of this compensation inductance is $L_{comp} = L_{drain} + L_{source}$, the compensation voltage created on this inductance is exactly the same as the sum of error voltages created on drain and source parasitic inductances i.e. $VL_{drain} + Vl_{source}$. The internal analog inverter (Figure 39) inverts compensation voltage Vl_comp and offsets the current sense comparator turn−off threshold. The current sense comparator thus “sees” between its terminals a voltage that would be seen on the SR MOSFET channel resistance in case the lead inductances wouldn’t exist. The current sense comparator of the NCP4304A/B is thus able to detect the secondary current zero crossing very precisely. More over, the secondary current turn−off threshold is then di(t)/t independent thus the NCP4304A/B allows to increase operating frequency of the SR system. One should note that the parasitic resistance of compensation inductance should

be as low as possible compared to the SR MOSFET channel and leads resistance otherwise compensation is not efficient. Typical value of compensation inductance for a TO−220 package is 7 nH. Waveforms from the application with compensated SR system can be seen in Figure 43. One can see the conduction time has been significantly increased and turn−off current reduced.

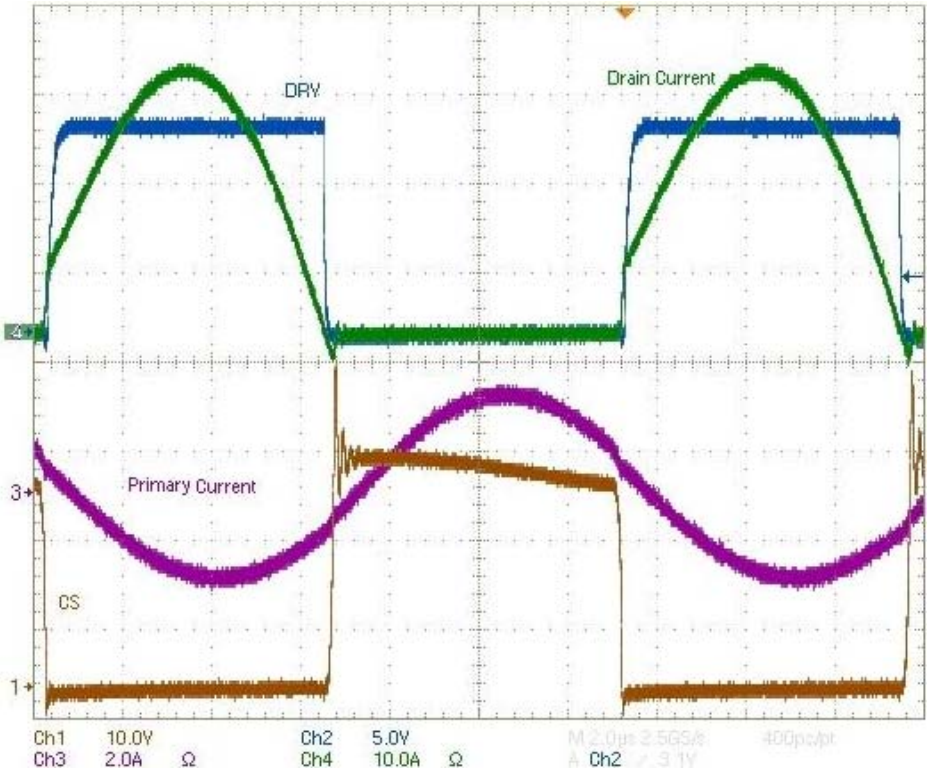


Figure 43. Waveforms SR System Using MOSFET in TO−220 Package with Parasitic Inductance Compensation – SR MOSFET Channel Conduction Time is Optimized

Note that using the compensation system is only beneficial in applications that are using a low $R_{DS(on)}$ MOSFET in non−SMT package. Using the compensation method allows for optimized efficiency with a standard TO220 package that in turn results in reduced costs, as the SMT MOSFETs usually require reflow soldering process and more expensive PCB.

From the above paragraphs and parameter tables it is evident that turn−off threshold precision is quite critical. If we consider a SR MOSFET with Rds_on of 1 mΩ, the 1 mV error voltage on the CS pin results in a 1 A turn−off current threshold difference. Thus the PCB layout is very critical when implementing the SR system. Note that the CS turn−off comparator as well as compensation inputs are referred to the GND pin. Any parasitic impedance (resistive or inductive − talking about mΩ and nH values) can cause a high error voltage that is then evaluated by the CS comparator. Ideally the CS turn−off comparator should detect voltage that is caused by secondary current directly on the SR MOSFET channel resistance. Practically this is not possible because of the bonding wires, leads and soldering. To assure the best efficiency results, a Kelvin connection of the SR controller to the power circuitry should be implemented (i.e. GND pin should be connected to the SR MOSFET source soldering point and current sense pin should be connected to the SR MOSFET drain soldering point). Any impact of PCB parasitic elements on the SR controller functionality is then avoided. Figures 44 and 45 show examples of SR system layouts using parasitic inductance compensation (i.e. for low $R_{DS(on)}$ MOSFET in TO−220 package) and not using compensation (i.e. for higher $R_{DS(on)}$ MOSFET in TO−220 package or SMT package MOSFETs).

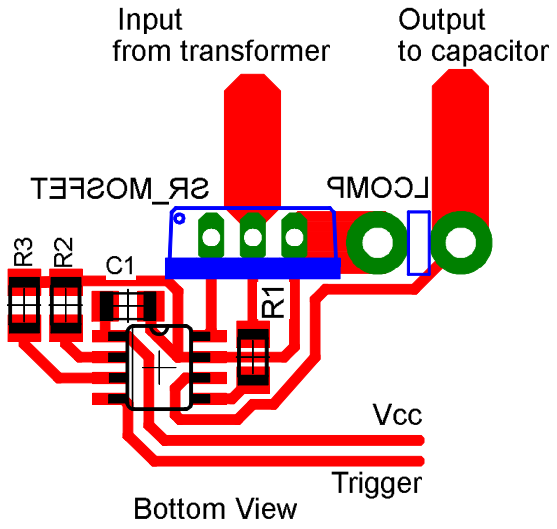


Figure 44. Recommended Layout When Parasitic Inductance Compensation is Used

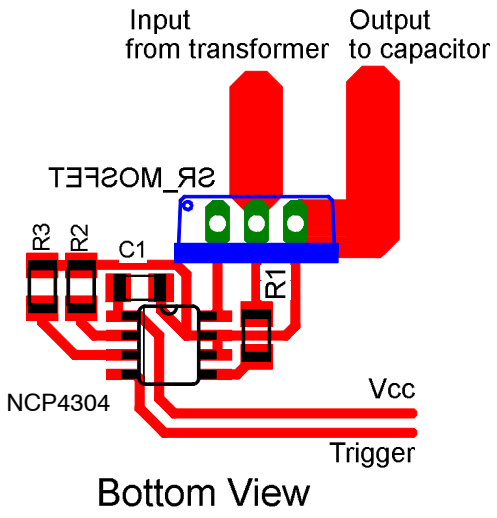


Figure 45. Recommended Layout When Parasitic Inductance Compensation is Not Used

Trigger/Disable input

The NCP4304A/B features an ultrafast trigger input that exhibits a typically of 10 ns delay from its activation to the turn−off of the SR MOSFET. The main purpose of this input is to turn-off the SR MOSFET in applications operating in CCM mode via a signal coming from the primary side or direct synchronization SR MOSFET turn−on and turn−off event according to primary controller signals. The NCP4304A/B operation can be disabled using the trigger/dis input. If the trigger/dis input is pulled high (above 2.5 V) the driver is disabled immediately, except during DRV rising edge when trigger/dis is blanked for 150 ns. If the trigger signal is high for more than 100 μs the driver enters standby mode. The IC consumption is reduced below 100 μA during the standby mode. The device recovers operation in 10 μs when the trigger voltage is increased to exit standby mode. Trigger/dis input is superior to CS input except blanking period. Trigger/dis signal turns−OFF the SR MOSFET or disable its turn−ON if trigger/dis is pulled above V_{trig}.

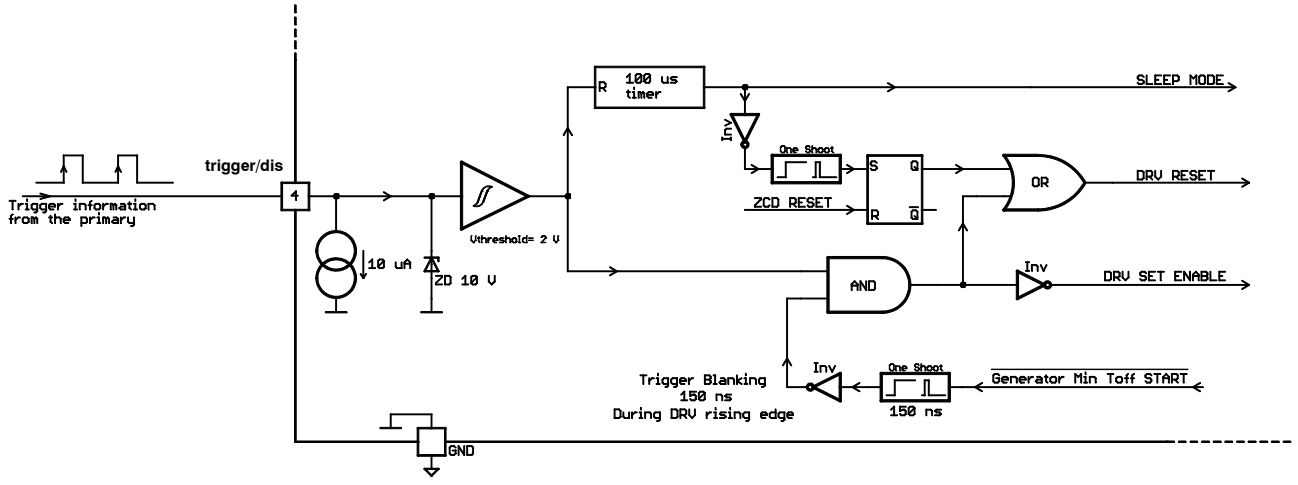


Figure 46. Trigger Input Internal Circuitry

Figure 47 depicts driver turn−ON events. Turn−ON of the SR MOSFET is possible if CS (Vds) signal falls under $V_{th\_cs\_ON}$ threshold and trigger/dis is pulled LOW (t1 to t3 time interval).

When the CS (Vds) reached the $V_{th\_cs\_ON}$ threshold and trigger/dis is pulled HIGH the driver stays LOW (t6, t7 time markers) if the trigger/dis is HIGH. If the trigger/dis is pulled LOW and CS (Vds) is still under $V_{th\_cs\_ON}$ threshold then the DRV is turned−ON (t7 marker).

Time markers t14 and t15 in Figure 47 demonstrate situation when CS (Vds) is above $V_{th\_cs\_ON}$ threshold and trigger/dis is pulled down. In this case the driver stays LOW (t12 to t15 marker).

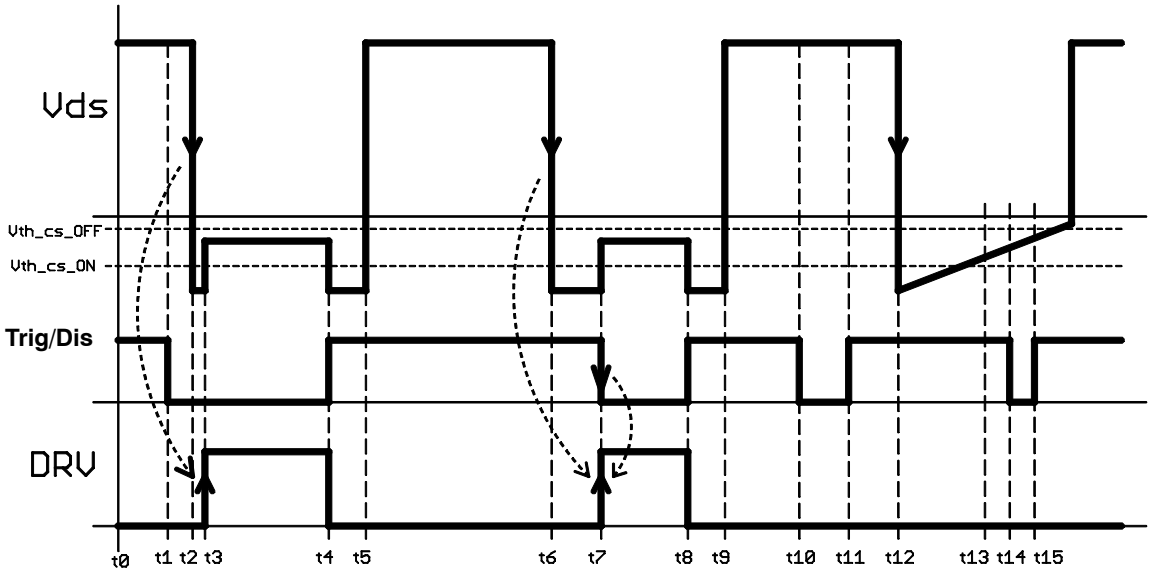


Figure 47. DRV Turn ON Events

The trigger/dis input is blanked for 150 ns after DRV set signal to avoid undesirable behavior during SR MOSFET turn−ON event. The blanking time in combination with high threshold voltage (2 V) prevent triggering on ringing and spikes that are present on the trigger/dis input pin during the SR MOSFET turn−on process. DRV response to the short needle pulse on the trigger/dis pin is depicted in Figure 48 – this short pulse turns−on the DRV for 150 ns.

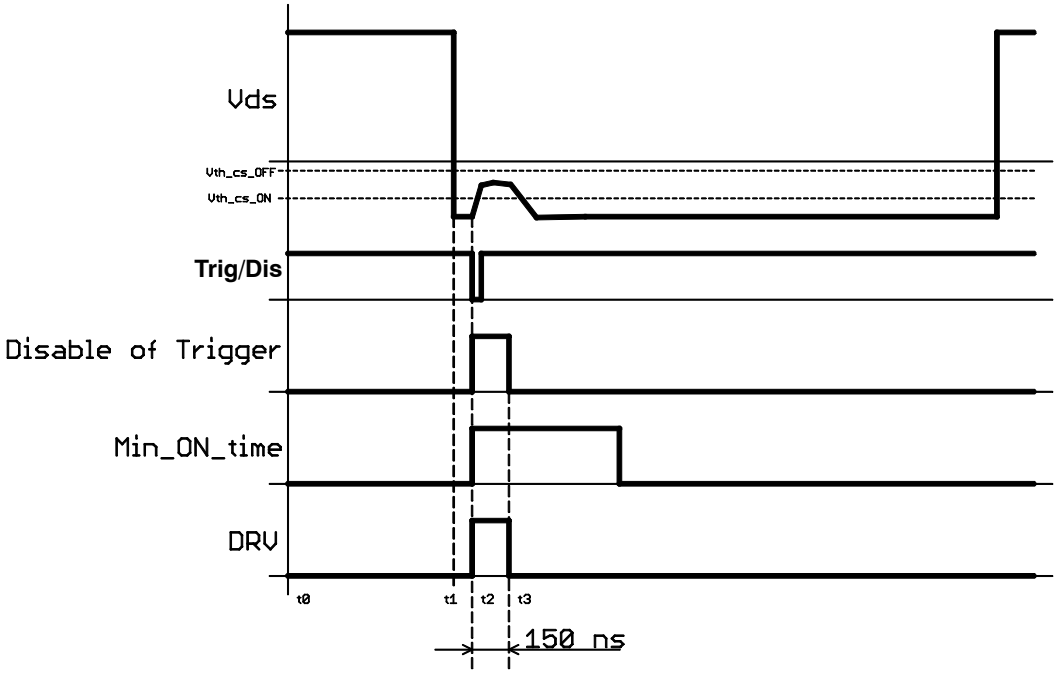


Figure 48. Trigger Needle Pulse and Trigger Blank Sequence

Advantage of the trigger blanking time during DRV turn−ON event is evident from Figure 49. Rising edge of the DRV signal may cause additional spikes on the trigger/dis input. These spikes, in combination with ultra−fast performance of the trigger logic, could turn−OFF the SR MOSFET in inappropriate time. Implementation of the trigger blanking time period helps to avoid such situation.

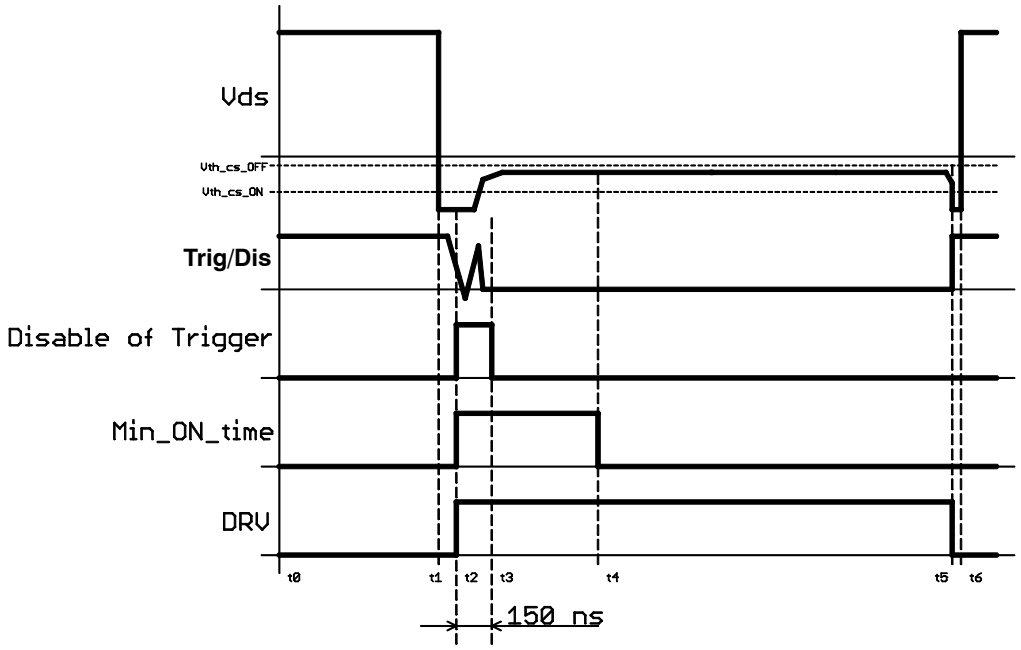


Figure 49. Trigger Blanking Masked−out Noise in Trigger Signal During Switch−ON Event

Figure 50 depicts driver turn−OFF events in details. If the CS (V_{ds}) stays below $V_{th\_cs\_OFF}$ threshold driver is turned−OFF according to rising edge of the trigger/dis signal. Trigger/dis can turn−OFF the driver also during minimum−ON time period (time marker t2 and t3 in Figure 50).

Figure 51 depicts another driver turn−OFF events in details. Driver is turned−OFF according to the CS (V_{ds}) signal (t2 marker) and only after minimum−ON time elapsed. Trigger/dis signal needs to be LOW during this event. If the CS (V_{ds}) voltage reaches Vth_cs_OFF threshold before minimum−ON time period ends and trigger/dis pin is LOW the DRV is turned−OFF on the falling edge of the minimum−ON time period (t4 and t6 time markers in Figure 51).

Figure 52 depicts performance of the NCP4304A/B controller when trigger pin is permanently pulled LOW. In this case the DRV is turned ON and OFF according to the CS (V_{ds}) signal. The driver can be turned off only after minimum−ON time period elapsed. The driver is turned−ON in the time when CS (Vds) reaches $V_{th\_cs\_ON}$ threshold (t1− t2, t5 – t6, t9 – t10 markers). DRV is turned−OFF if CS (V_{ds}) signal reaches $V_{th\_cs\_OFF}$ threshold (t4 marker). The DRV ON−time is prolonged till minimum−ON time period falling edge if the CS (Vds) reaches $V_{th\_cs\_OFF}$ before minimum−ON time period elapsed (t7 – t8, t11 – t12 markers).

Figure 53 depicts entering into the sleep mode. If the trigger/dis is pulled up for more than 100 μs the NCP4304A/B enters low consumption mode. The DRV stays LOW (disabled) during entering sleep mode.

Figure 54 shows sleep mode transition 2nd case – i.e. trigger rising edge comes during the trigger blank period.

Figure 55 depicts entering into sleep mode and wake−up sequence.

Figures 56 and 57 show wake−up situations in details. If the NCP4304A/B is in sleep mode and Trigger/dis is pulled LOW NCP4304A/B requires up to 10 μs period to recover all internal circuitry to normal operation mode. The driver is then enabled in the next cycle of CS (Vds) signal only. The DRV stays LOW during waking−up time period.

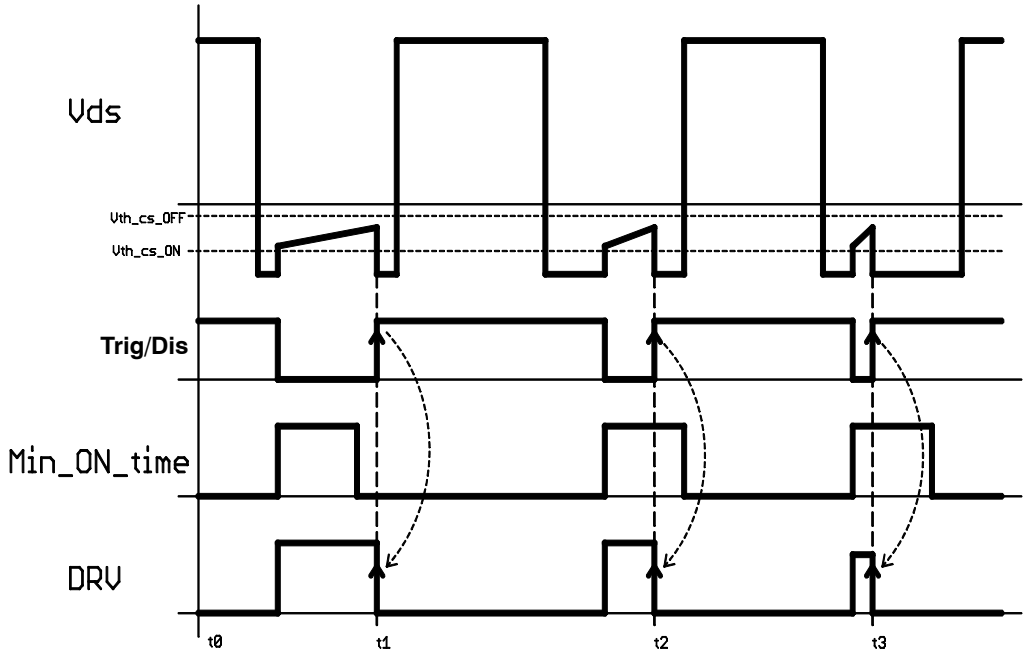


Figure 50. Driver Turn−OFF Events Based on the Trigger Input

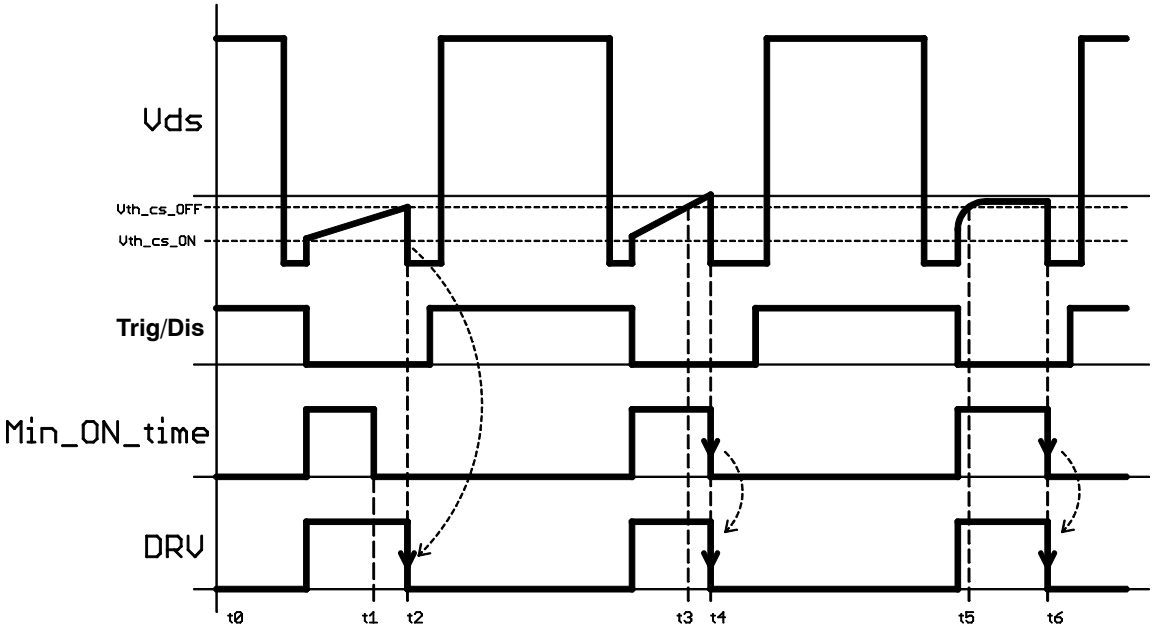


Figure 51. Driver OFF Sequence Chart 2

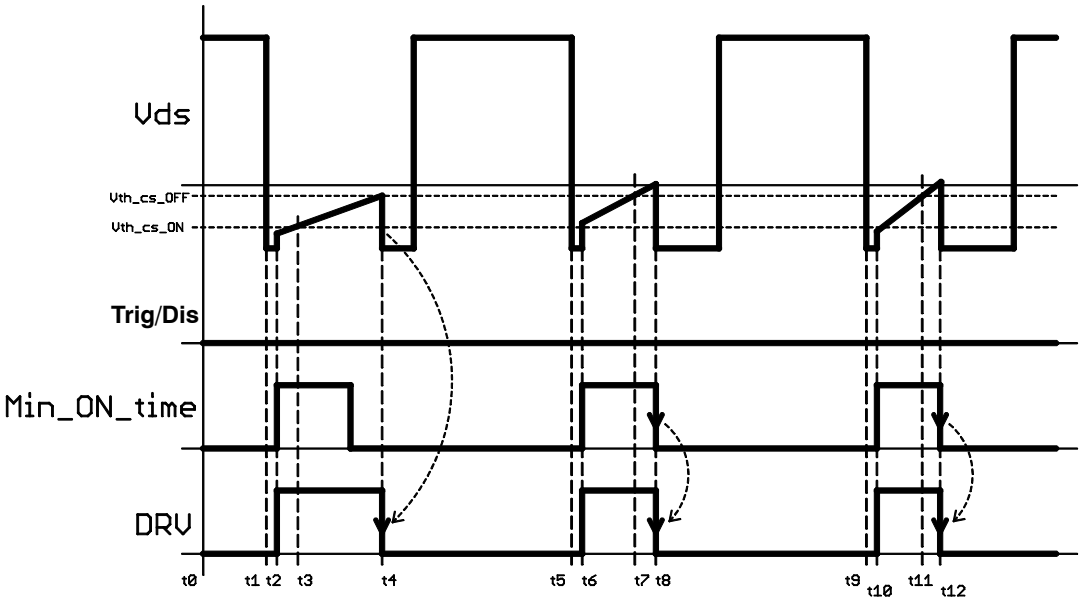


Figure 52. Trigger/dis is HIGH Sequence Chart

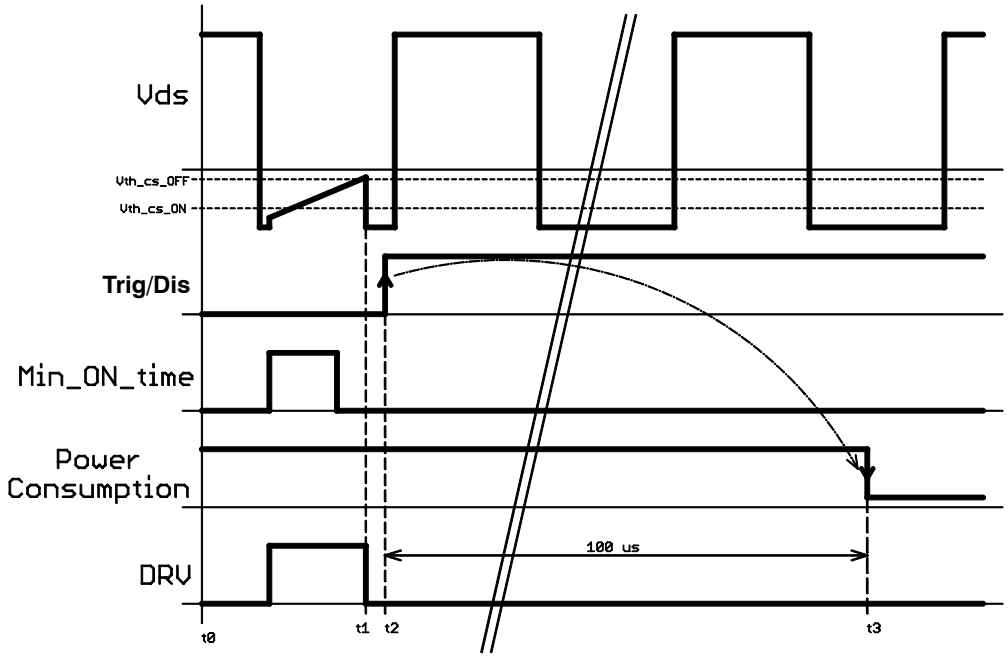


Figure 53. Trigger/dis form HIGH to LOW Sequence 1

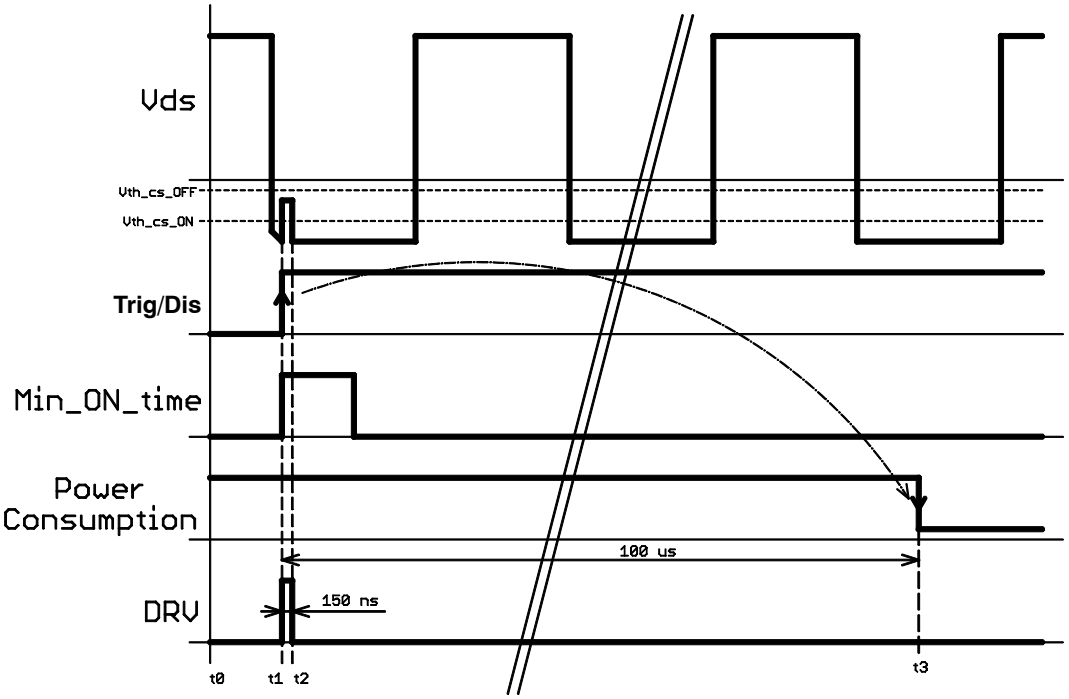


Figure 54. Trigger/dis form HIGH to LOW Sequence 2

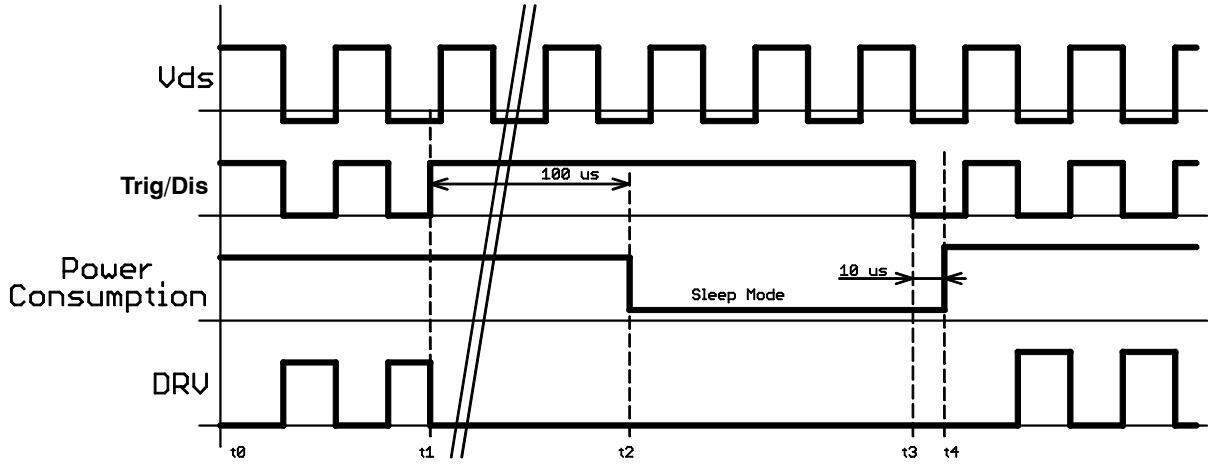


Figure 55. Sleep Mode Sequence

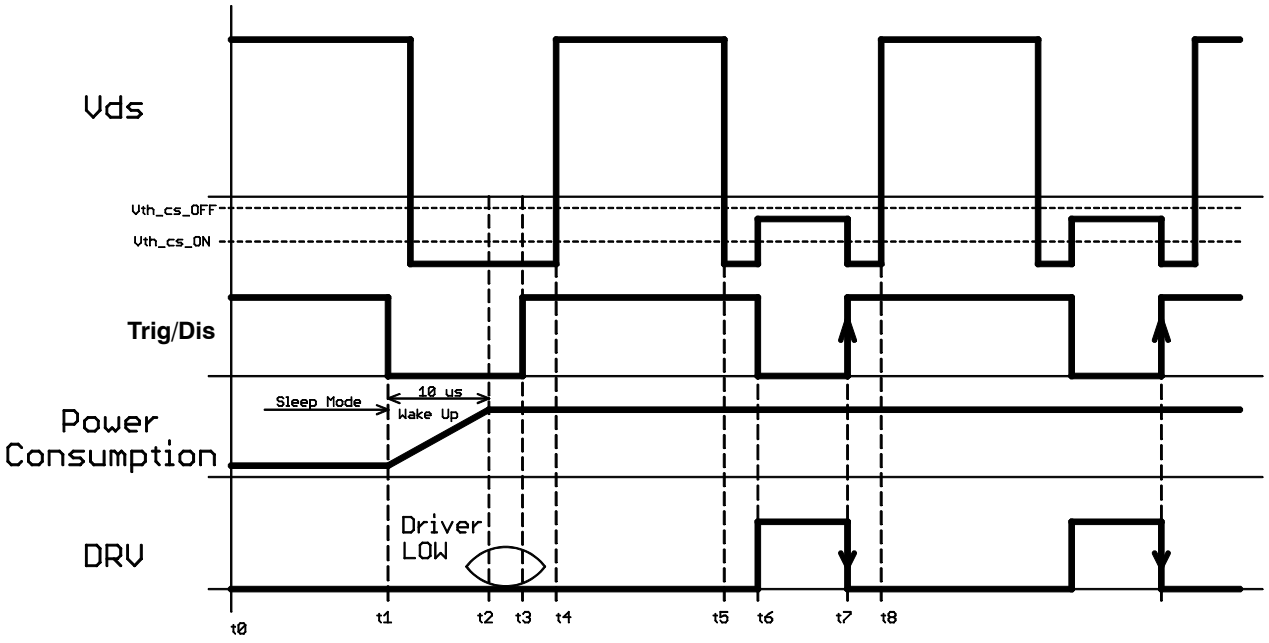


Figure 56. Waking−up Sequence

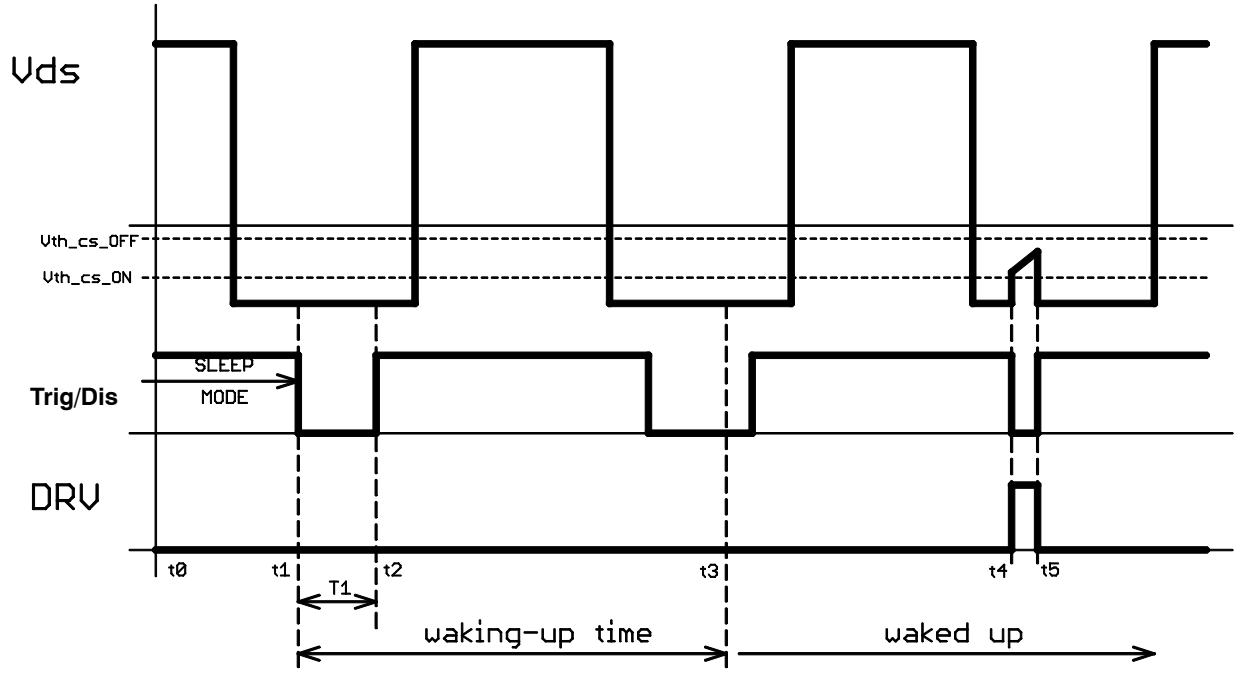


Figure 57. Wake−up Time Sequence

Figure 58 shows IC behavior in case the trigger signal features two pulses during one cycle of the V_{ds} (CS) signal. Trigger enables driver at time t1 and DRV turns ON because the V_{ds} voltage is under $V_{th\_cs\_ON}$ threshold voltage. The trigger signal and consequently DRV output fall down in time t2. The minimum OFF time generator is triggered in time t2. Trigger drops down to LOW level in time t3 but there is still minimum OFF time sequence present so the DRV output stays low. When the minimum OFF time sequence elapses in time t4 the DRV is turned ON. In time t5 Trigger signal rises up and terminates this cycle of the CS signal in time t5. Next cycle starts in time t6. Trigger enables DRV and V_{ds} is under $V_{th\_cs\_ON}$ threshold voltage so DRV turns ON in time t6. Trigger signal rises up to HIGH level in time t7, consequently DRV turns OFF and this starts minimum OFF time generator. Because minimum OFF time period is longer then the rest of time to the end of cycle of V_{ds} − DRV is disabled.

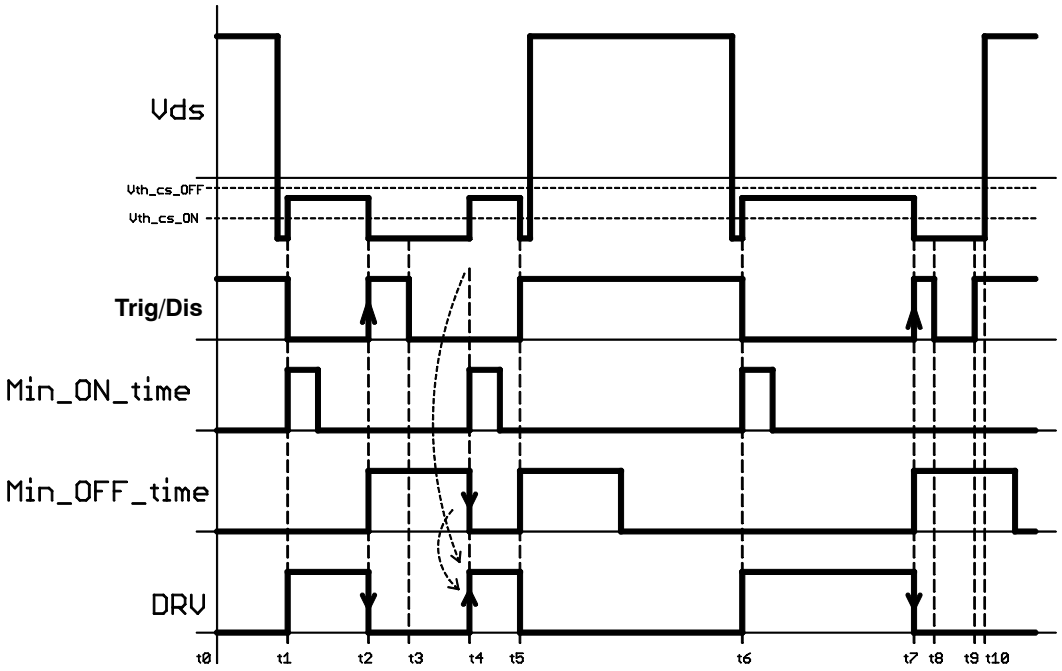


Figure 58. IC Behavior When Multiple Trigger Pulses Appear on Trigger Input

Note that the trigger input is an ultrafast input that is sensitive even to very narrow voltage pulses. Thus it is wise to keep this input on a low impedance path and provide it with a clean triggering signal in the time this input is enabled by internal logic.

A typical application schematic of a CCM flyback converter with the NCP4304A/B driver can be seen in Figure 59. In this application the trigger signal is taken directly from the flyback controller driver output and transmitted to the secondary side by pulse transformer TR2. Because the trigger input is edge sensitive, it is not necessary to transmit the entire primary driver pulse to the secondary. The coupling capacitor C5 is used to allow pulse transformer core reset and also to prepare a needle pulse (a pulse with width lower than 100 ns) to be transmitted to the NCP4304A/B trigger input. The advantage of needle trigger pulse usage is that the required volt−second product of the pulse transformer is very low and that allows the designer to use very small and cheap magnetics. The trigger transformer can be for instance prepared on a small toroidal ferrite core with diameter of 8 mm. Proper safety insulation between primary and secondary sides can be easily assured by using triple insulated wire for one or even both windings.

The primary MOSFET gate voltage rising edge is delayed by external circuitry consisting of transistors Q1, Q2 and surrounding components. The primary MOSFET is thus turned−on with a slight delay so that the secondary controller turns−off the SR MOSFET by trigger signal prior to the primary switching. This method reduces the commutation losses and the SR MOSFET drain voltage spike, which results in improved efficiency.

It is also possible to use capacitive coupling (use additional capacitor with safety insulation) between the primary and secondary to transmit the trigger signal. We do not recommend this technique as the parasitic capacitive currents between primary and secondary may affect the trigger signal and thus overall system functionality.

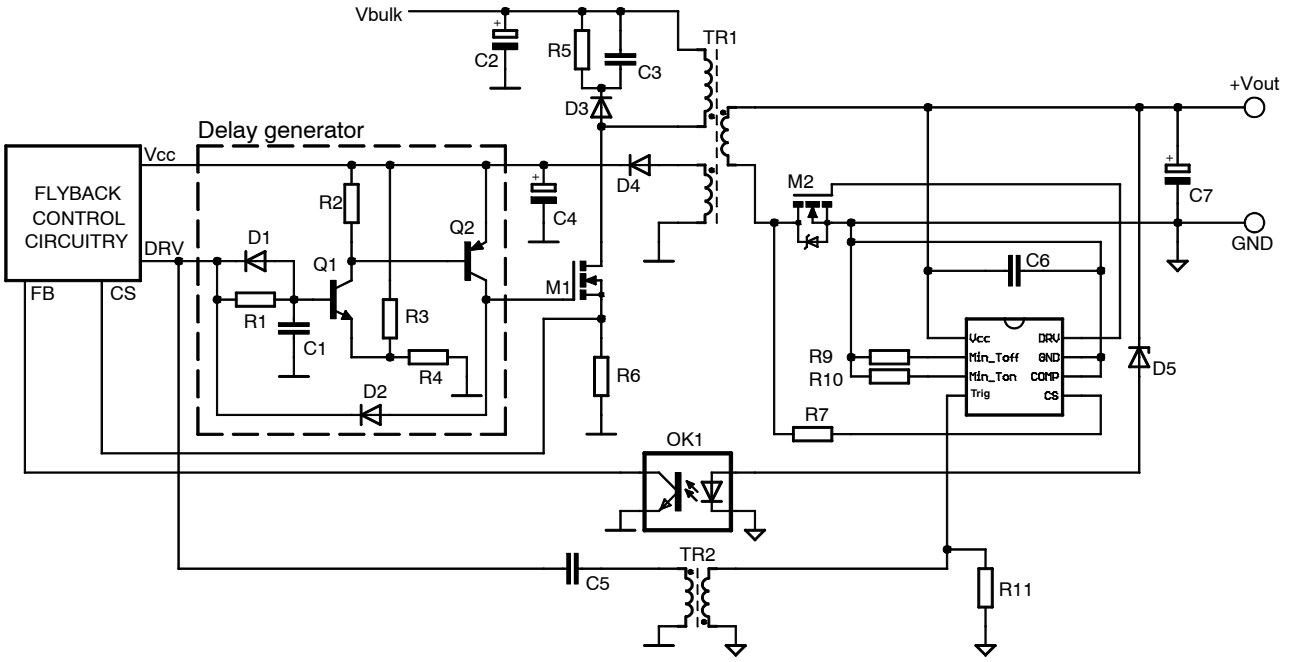


Figure 59. Typical Application Schematic when NCP4304A/B is Used in CCM Flyback Converter

Minimum T_{on} and T_{off} Adjustment

The NCP4304A/B offers adjustable minimum ON and OFF time periods that ease the implementation of the synchronous rectification system in a power supply. These timers avoid false triggering on the CS input after the MOSFET is turned on or off. The adjustment is based on an internal timing capacitance and external resistors connected to the GND pin – refer to Figure 60 for better understanding.

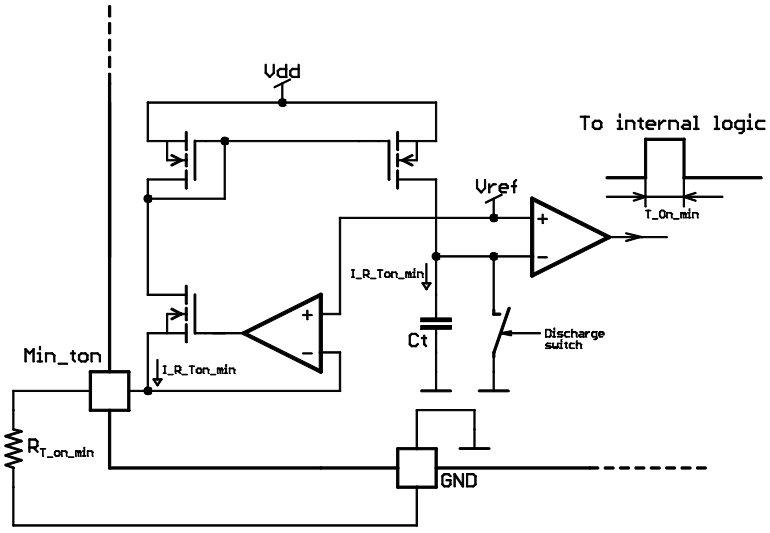


Figure 60. Internal Circuitry of $MIN_{Ton\_generator}$ ($MIN_{Toff\_generator}$ works in the same way)

Current through the Min_ton adjust resistor can be calculated as:

$$I_{R\_Ton\_min} = \frac{V_{ref}}{R_{Ton\_min}} \qquad \text{(eq. 4)}$$

As the same current is used for the internal timing capacitor (Ct) charging, one can calculate the minimum on−time duration using this equation.

$$T_{on\_min} = C_t \cdot \frac{V_{ref}}{I_{R\_Ton\_min}} = C_t = \frac{V_{ref}}{\frac{V_{ref}}{R_{Ton\_min}}} \qquad \text{(eq. 5)}$$

$$= C_t \cdot R_{Ton\_min}$$

As can be seen from Equation 5, the minimum ON and OFF times are independent of the Vref or Vcc level. The

internal capacitor size would be too high if we would use directly $I_{R\_Ton\_min}$ current thus this current is decreased by the internal current mirror ratio. One can then calculate the minimum T_{on} and T_{off} blanking periods using below equations:

$$T_{on\_min} = 9.82 * 10^{-11} * R_{T\_on\_min} + 4.66 * 10^{-8} \ [\mu s] \quad \text{(eq. 6)}$$

$$T_{off\_min} = 9.56 * 10^{-11} * R_{T\_off\_min} + 5.397 * 10^{-8} \ [\mu s] \quad \text{(eq. 7)}$$

Note that the internal timing comparator delay affects the accuracy of equations Equations 6 and 7 when minimum T_{on}/T_{off} times are selected near to their minimum possible values. Please refer to Figure 61 and 62 for measured minimum on and off time charts.

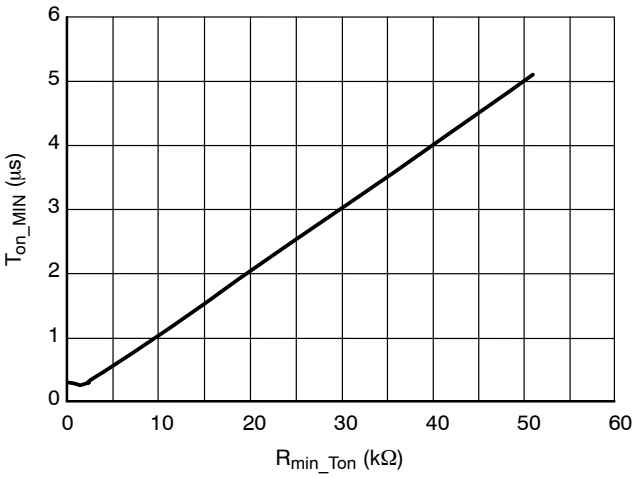


Figure 61. Min_Ton Adjust Characteristic

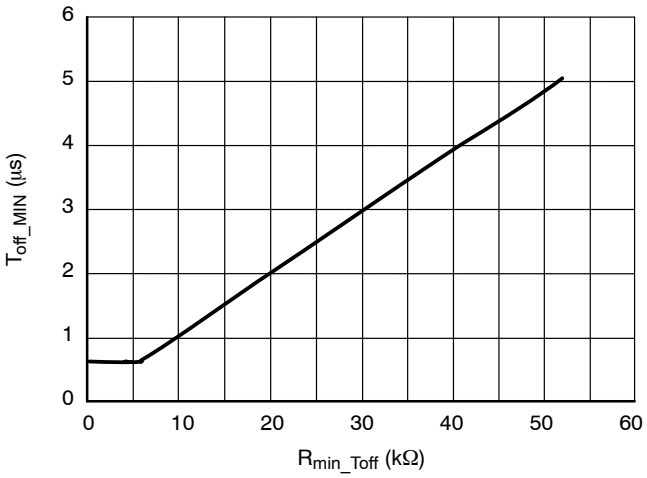


Figure 62. Min_Toff Adjust Characteristic

The absolute minimum T_{on} duration is internally clamped to 300 ns and minimum T_{off} duration to 600 ns in order to prevent any potential issues with the minimum Ton and/or T_{off} input being shorted to GND.

Some applications may require adaptive minimum on and off time blanking periods. With NCP4304A/B it is possible to modulate blanking periods by using an external NPN transistor – refer to Figure 63. The modulation signal can be derived based on the load current or feedback regulator voltage.

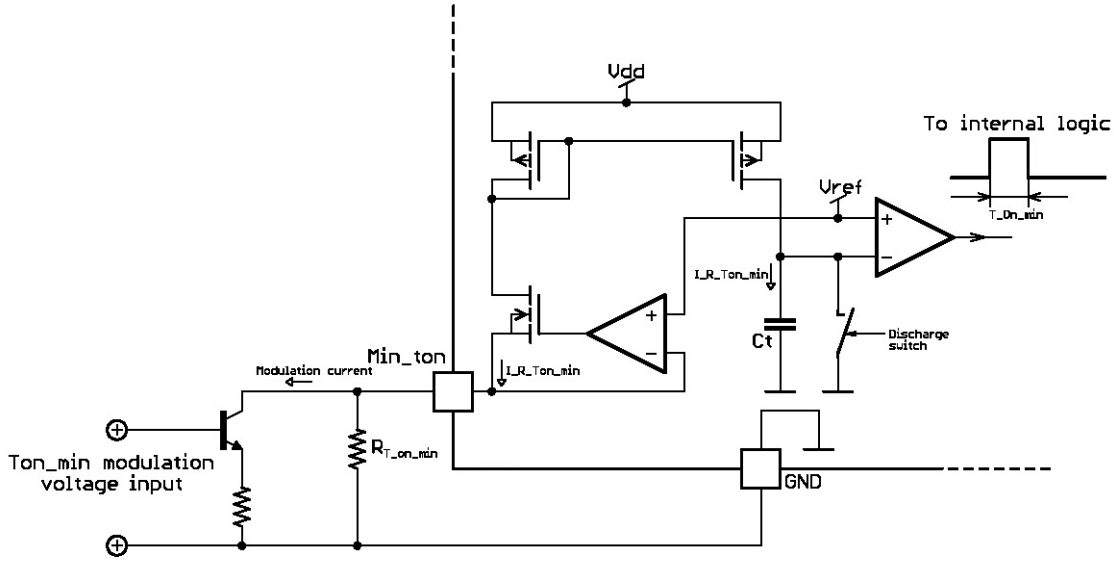


Figure 63. Possible Connection for Min T_on and Min T_off Modulation

In LLC applications with a very wide operating frequency range it is necessary to have very short minimum on time and off time periods in order to reach the required maximum operating frequency. However, when a LLC converter operates under low frequency, the minimum off time period may then be too short. To overcome possible issues with the LLC operating under low line and light load conditions, one can prolong the minimum off time blanking period by using resistors R_{drain1} and R_{drain2} connected from the opposite SR MOSFET drain – refer to Figure 64.

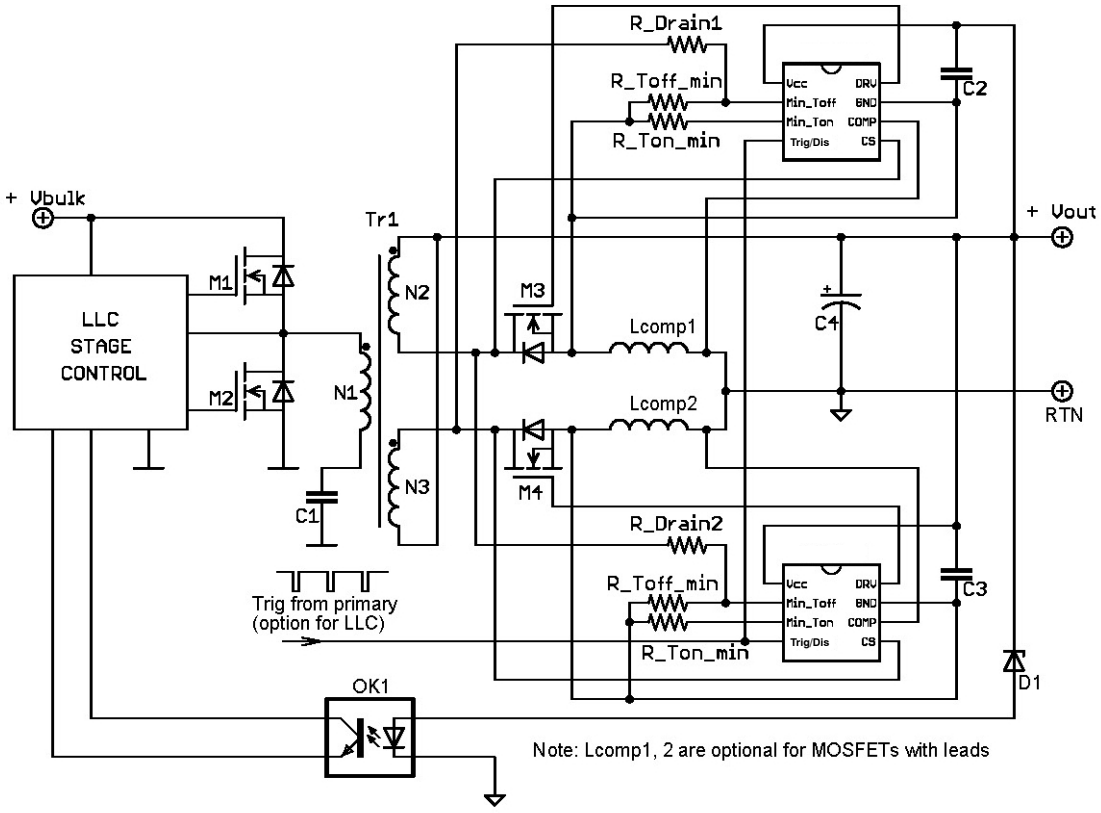


Figure 64. Possible Connection for Min Toff Prolongation in LLC Application with Wide Operating Frequency Range

Note that R_{drain1} and R_{drain2} should be designed in such a way that the maximum pulse current into the Min_Toff adjust pin is below 10 mA. Voltage on the min Toff and Ton pins is clamped by internal zener protection to 10 V.

Power Dissipation Calculation

It is important to consider the power dissipation in the MOSFET driver of a SR system. If no external gate resistor is used and the internal gate resistance of the MOSFET is very low, nearly all energy losses related to gate charge are dissipated in the driver. Thus it is necessary to check the SR driver power losses in the target application to avoid over temperature and to optimize efficiency.

In SR systems the body diode of the SR MOSFET starts conducting before turn on because the $V_{th\_cs\_on}$ threshold level is below 0 V. On the other hand, the SR MOSFET turn off process always starts before the drain to source voltage rises up significantly. Therefore, the MOSFET switch always operates under Zero Voltage Switching (ZVS) conditions when implemented in a synchronous rectification system.

The following steps show how to approximately calculate the power dissipation and DIE temperature of the NCP4304A/B controller. Note that real results can vary due to the effects of the PCB layout on the thermal resistance.

Step 1 – MOSFET Gate−to−Source Capacitance:

During ZVS operation the gate to drain capacitance does not have a Miller effect like in hard switching systems because the drain to source voltage is close to zero and its change is negligible.

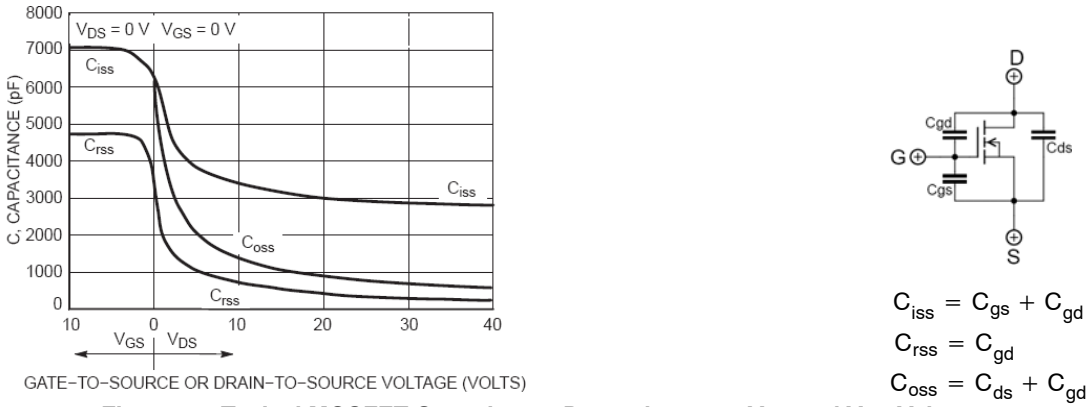


Figure 65. Typical MOSFET Capacitance Dependency on V_{DS} and V_{GS} Voltage

Therefore, the input capacitance of a MOSFET operating in ZVS mode is given by the parallel combination of the gate to source and gate to drain capacitances (i.e. C_{iss} capacitance for given gate to source voltage). The total gate charge, Q_{g_total}, of most MOSFETs on the market is defined for hard switching conditions. In order to accurately calculate the driving losses in a SR system, it is necessary to determine the gate charge of the MOSFET for operation specifically in a ZVS system. Some manufacturers define this parameter as Q_{g_ZVS}. Unfortunately, most datasheets do not provide this data. If the C_{iss} (or Q_{g_ZVS}) parameter is not available then it will need to be measured. Please note that the input capacitance is not linear (as shown Figure 65) and it needs to be characterized for a given gate voltage clamp level.

Step 2 – Gate Drive Losses Calculation:

Gate drive losses are affected by the gate driver clamp voltage. Gate driver clamp voltage selection depends on the type of MOSFET used (threshold voltage versus channel resistance). The total power losses (driving loses and conduction losses) should be considered when selecting the gate driver clamp voltage. Most of today's MOSFETs for SR systems feature low $R_{DS(on)}$ for 5 V V_{gs} voltage and thus it is beneficial to use the B version. However, there is still a big group of MOSFETs on the market that require higher gate to source voltage – in this case the A version should be used.

The total driving loss can be calculated using the selected gate driver clamp voltage and the input capacitance of the MOSFET:

$$P_{DRV\_total} = V_{CC} \cdot V_{clamp} \cdot C_{g\_ZVS} \cdot f_{SW} \quad \text{(eq. 8)}$$

Where:

V_{CC}	is the supply voltage
V_{clamp}	is the driver clamp voltage
C_{g_ZVS}	is the gate to source capacitance of the MOSFET in ZVS mode
f_{sw}	is the switching frequency of the target application

The total driving power loss won't only be dissipated in the IC, but also in external resistances like the external gate resistor (if used) and the MOSFET internal gate resistance (Figure 66). Because NCP4304A/B features a clamped driver, it's high side portion can be modeled as a regular driver switch with equivalent resistance and a series voltage source. The low side driver switch resistance does not drop immediately at turn−off, thus it is necessary to use an equivalent value ($R_{drv\_low\_eq}$) for calculations. This method simplifies power losses calculations and still provides acceptable accuracy. Internal driver power dissipation can then be calculated using Equation 9:

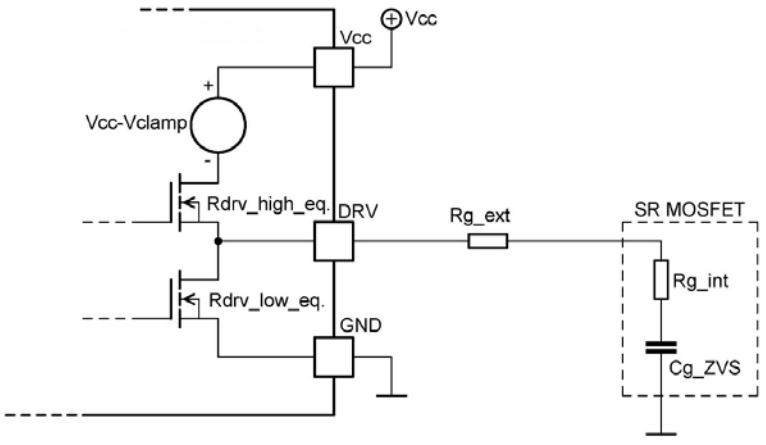


Figure 66. Equivalent Schematic of Gate Drive Circuitry

$$P_{DRV\_IC} = \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{clamp}{}^2 \cdot f_{SW} \cdot \left(\frac{R_{drv\_low\_eq}}{R_{drv\_low\_eq} + R_{g\_ext} + R_{g\_int}} \right) + C_{g\_ZVS} \cdot V_{clamp} \cdot f_{SW} \cdot \left(V_{CC} - V_{clamp} \right)$$

(eq. 9)

$$+ \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{clamp}{}^2 \cdot f_{SW} \cdot \left(\frac{R_{drv\_high\_eq}}{R_{drv\_high\_eq} + R_{g\_ext} + R_{g\_int}} \right)$$

Where:

$R_{drv\_low\_eq}$ is the Ddriver low side switch equivalent resistance (1.55 Ω)

$R_{drv\_high\_eq}$ is the driver high−side switch equivalent resistance (7 Ω)

R_{g_ext} is the external gate resistor (if used)

R_{g_int} is the internal gate resistance of the MOSFET

Step 3 – IC Consumption Calculation:

In this step, power dissipation related to the internal IC consumption is calculated. This power loss is given by the I_{CC} current and the IC supply voltage. The I_{CC} current depends on switching frequency and also on the selected min Ton and Toff periods because there is current flowing out from the min Ton and Toff pins. The most accurate method for calculating these losses is to measure the I_{CC} current when C_{load} = 0 nF and the IC is switching at the target frequency with given min_Ton and min_Toff adjust resistors. Refer also to Figure 67 for typical IC consumption charts when the driver is not loaded. IC consumption losses can be calculated as:

$$P_{ICC} = V_{CC} \cdot I_{CC} \quad \text{(eq. 10)}$$

Step 4 – IC DIE Temperature Arise Calculation:

The DIE temperature can be calculated now that the total internal power losses have been determined (driver losses plus internal IC consumption losses). The SO−8 package thermal resistance is specified in the maximum ratings table for a 35 μm thin copper layer with no extra copper plates on any pin (i.e. just 0.5 mm trace to each pin with standard soldering points are used).

The DIE temperature is calculated as:

$$T_{DIE} = \left(P_{DRV\_IC} + P_{ICC} \right) \cdot R_{\theta J-A} + T_A \quad \text{(eq. 11)}$$

Where:

P_{DRV_IC} is the IC driver internal power dissipation

P_{Icc} is the IC control internal power dissipation

$R_{\theta JA}$ is the thermal resistance from junction to ambient

T_A is the ambient temperature

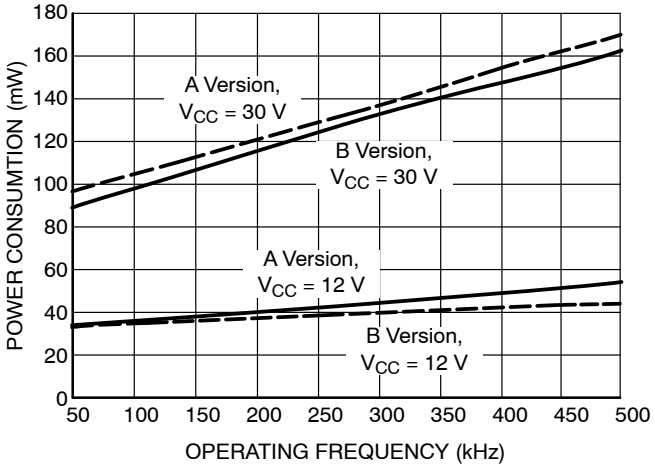


Figure 67. IC Power Consumption as a Function of Frequency for C_{load} = 0 nF, $R_{Ton\ min} = R_{Toff\ min}$ = 5 kΩ

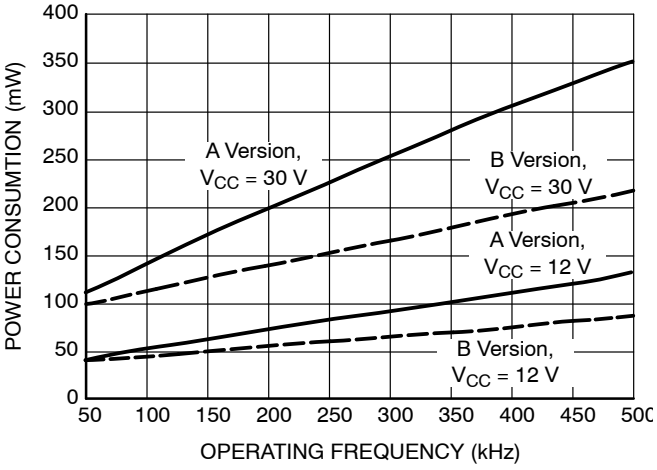


Figure 68. IC Power Consumption as a Function of Frequency for C_{load} = 1 nF, $R_{Ton\ min} = R_{Toff\ min}$ = 5 kΩ

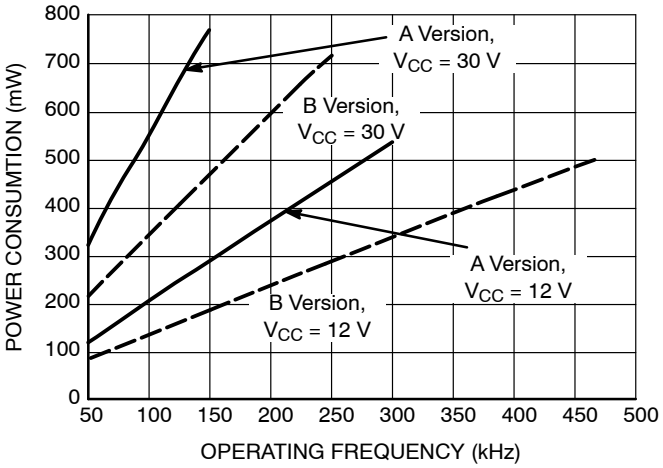
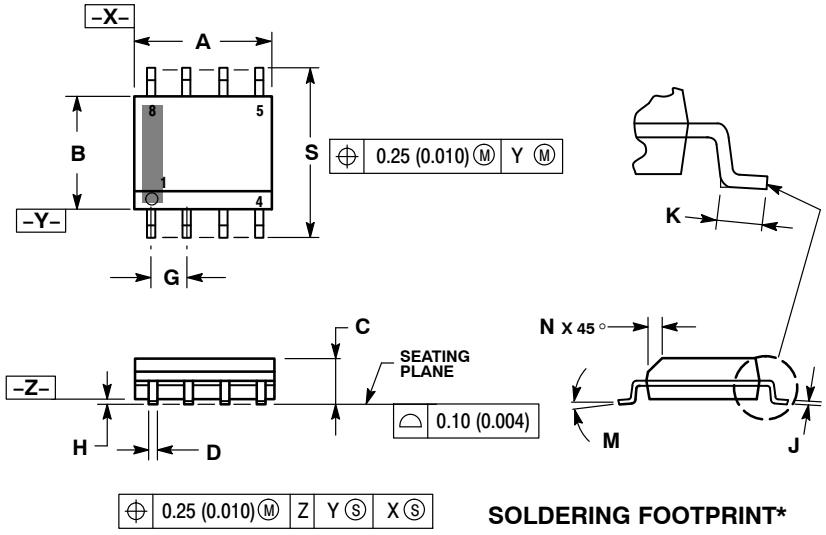


Figure 69. IC Power Consumption as a Function of Frequency for C_{load} = 10 nF, R_{Ton_min} = R_{Toff_min} = 5 kΩ

PACKAGE DIMENSIONS

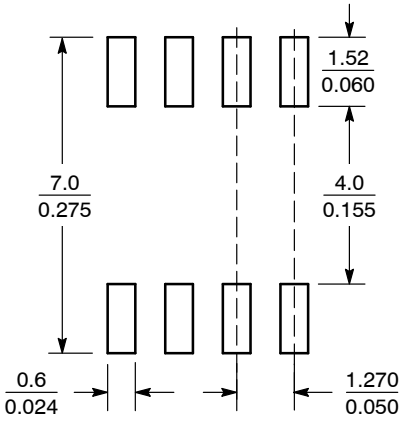
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

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CASE 488AF−01
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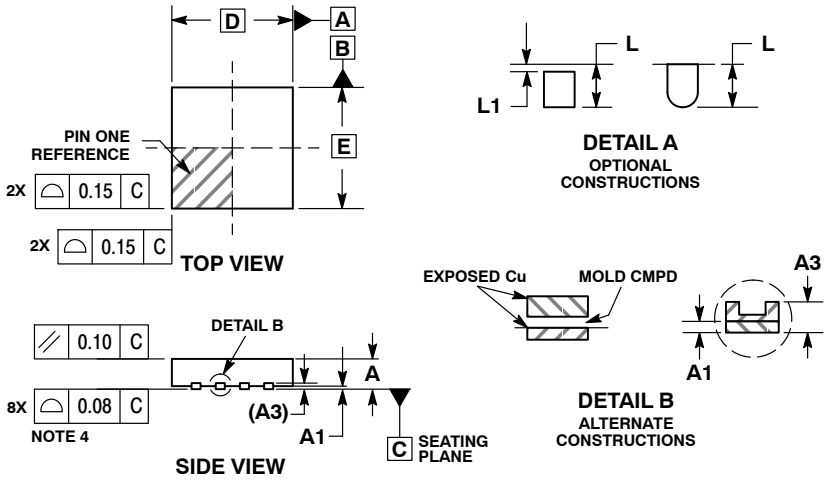
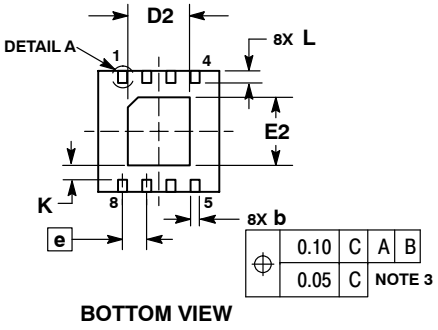
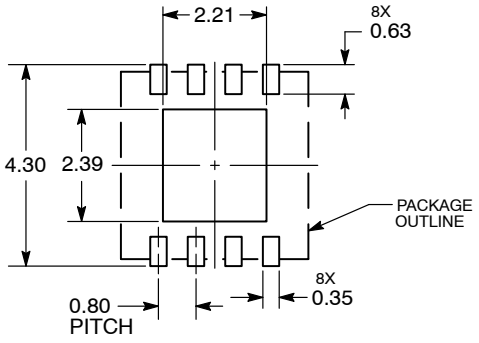


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	−−−
L	0.30	0.50
L1	−−−	0.15



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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