SEVEN CHANNEL RC DECODER — NE5045

DESCRIPTION

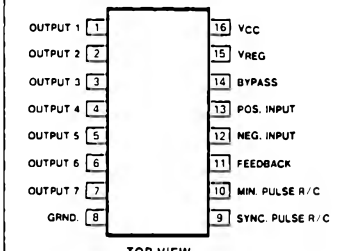
The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $T_W = R_S C_S$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver providing excellent isolation from the power supply as well as the decoder logic.

APPLICATIONS

- **Radio controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**
- **Robotics**
- **Telemetry**

PIN CONFIGURATION

D,N PACKAGE



TOP VIEW

ORDER NUMBERS

NE5045N NE5045D

FEATURES

- **Decodes up to 7 channels**
- **High gain input amplifier**
- **Externally set sync. pause and minimum pulse**
- **Wide supply voltage range, 3.6V–8V.**
- **Positive or negative pulse inputs**
- **Noise and flutter rejection**
- **Outputs reset to zero without inputs**
- **Compatible with all transmission mediums**

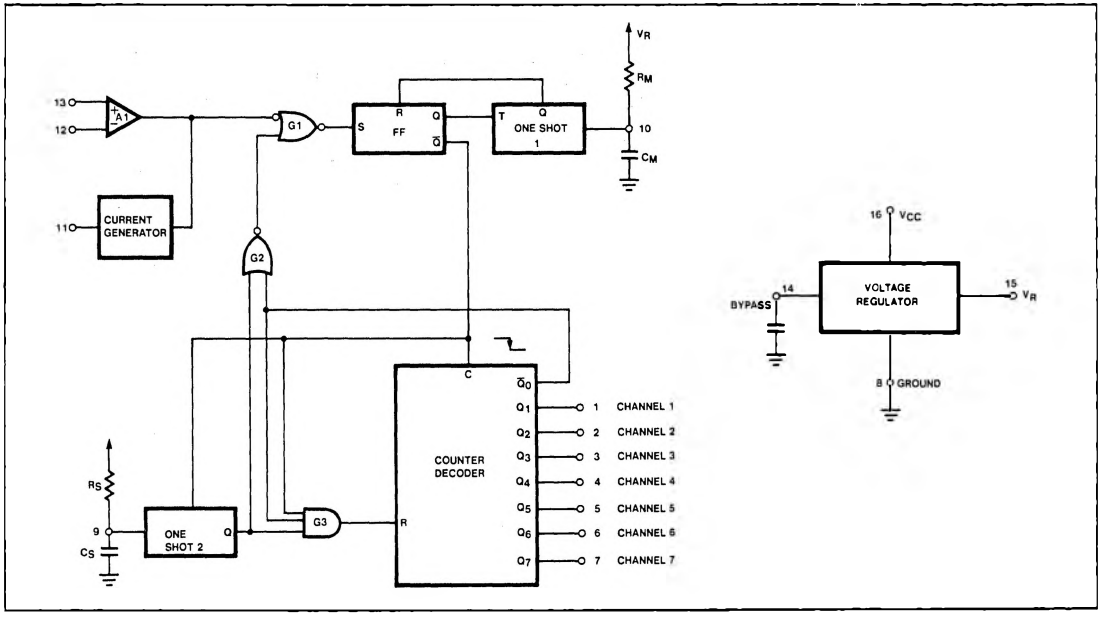
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	10	V
Regulator output current	−25	mA
Decoded output current	±5	mA
Pause input voltage	0 to V_R	V
Input amplifier voltage	0 to V_R	V
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE

1. T_A = 25°C unless otherwise stated

BLOCK DIAGRAM

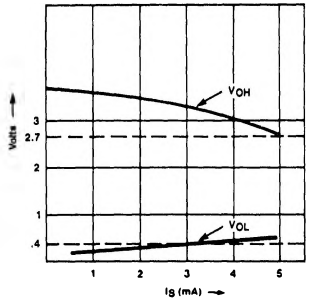


SEVEN CHANNEL RC DECODER — NE5045

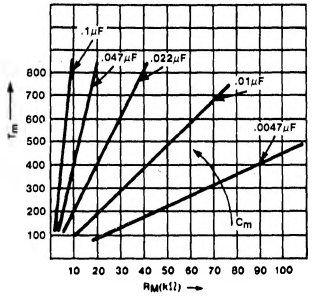
DC ELECTRICAL CHARACTERISTICS Standard conditions: (T_A = 25°C, V_{CC} = 5.0V unless otherwise stated), using Test Circuit #1

	PARAMETER	TEST CONDITIONS	NE5045 Min	NE5045 Typ	NE5045 Max	UNIT
	POWER SUPPLY REQUIREMENTS					
	Power supply voltage range	Test circuit #1	3.6		8.0	V
	Power supply current	Excluding input bias current		9.0	14.0	mA
	VOLTAGE REGULATOR					
	Output voltage		3.7	4.1	4.5	V
V_R	Output current	$V_R \geq 3.7V$			−15	mA
	Line regulation	V_{CC} = 6V to 8V		.01	.05	V/V
	Voltage drop	V_{CC} = 4V, I_R = −10mA			1.3	V
	INPUT AMPLIFIER					
	Input bias current			10	100	nA
	Input voltage range		2.0		4.0	V
	Open loop gain			60		dB
	Feedback current		100	200	400	μA
	Detection threshold	Test circuit #1, ΔV12 & 13		8	20	mV
T_S	Sync. pause time	$R_S C_S$ = 6.0ms	5.1	6.0	6.9	ms
T_M	Minimum pulse time	$R_m C_m$ = 500μs	405	475	545	μs
	OUTPUTS-ALL CHANNELS					
	V_{OL}	I_{SINK} = 1mA		.25	.5	V
	V_{OH}	I_{SOURCE} = 2mA	2.7			V

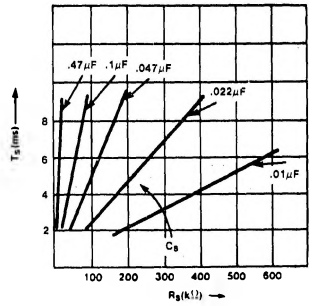
V_{OL} vs SINK CURRENT AND V_{OH} vs SOURCE CURRENT



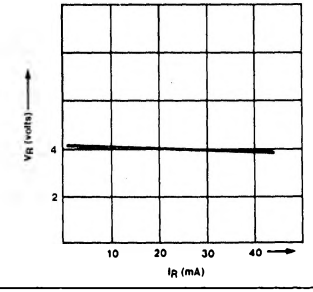
MINIMUM PULSE TIME, T_M vs R_M, C_M



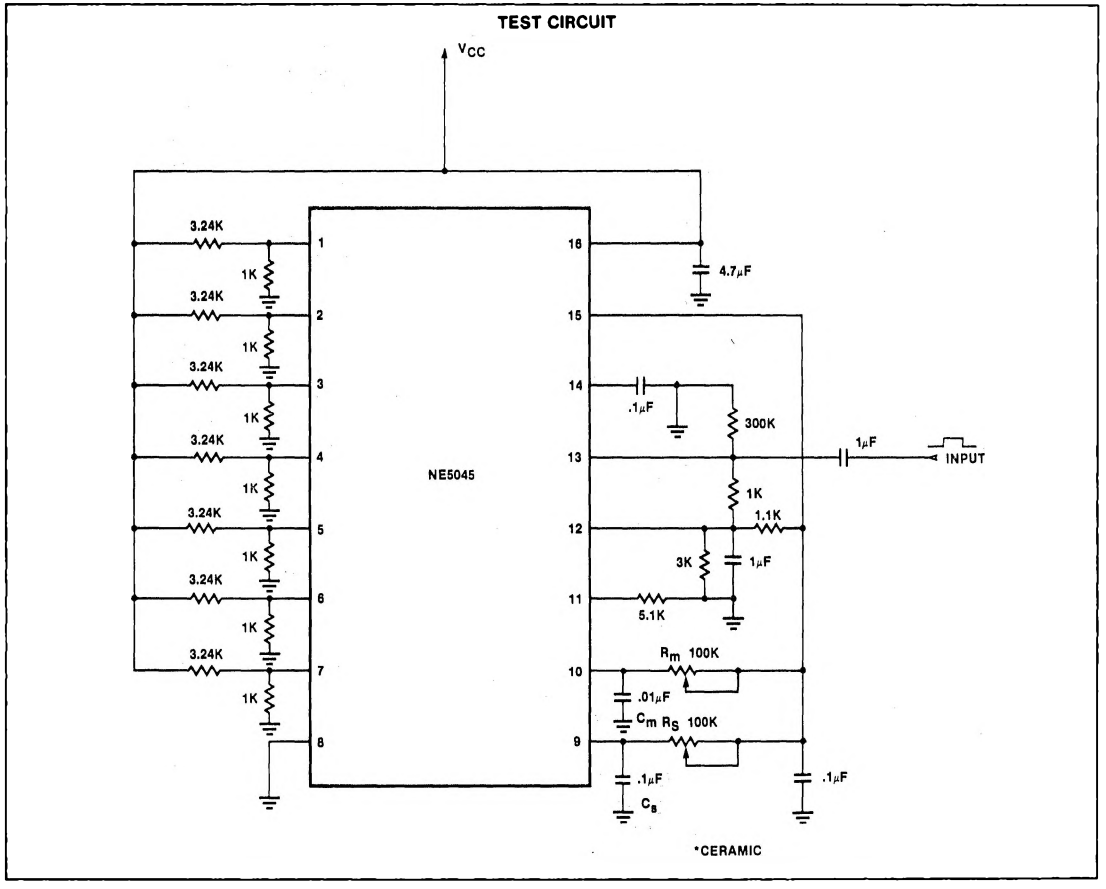
SYNC. PAUSETIME, T_S vs R_SC_S



REGULATOR VOLTAGE vs LOAD CURRENT



SEVEN CHANNEL RC DECODER — NE5045



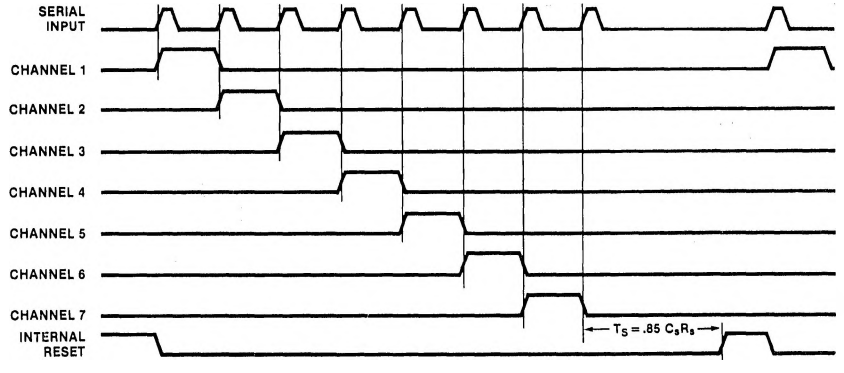


Figure 1. NE5045 Decoder Timing Diagram

SEVEN CHANNEL RC DECODER — NE5045

A. CIRCUIT OPERATION

The NE5045 is a serial input, parallel output decoder containing all the active circuitry necessary to separate up to 7 channels of information in a pulsewidth modulated system. An internal voltage regulator provides excellent power supply rejection for the decoder as well as a regulated output for a radio receiver if used.

The high gain input amplifier, A1 (A_v > 60dB), allows either positive or negative pulses to be used and has input bias currents less than 10nA. Signals as low as 10mV p-p can easily be demodulated. The feedback current generator can be used to provide positive feedback thereby creating hysteresis in the input switching levels. Hysteresis prevents false triggering due to noise or IF amplifier distortion. If positive input pulses are used, the signal would be connected to the noninverting input, pin 13. In this case, the input threshold would be set by the voltage difference between pin 12 and pin 13, established externally with a resistive divider network. Design of the divider will be covered in section B and C. Negative input signals would be coupled to pin 12, the inverting input.

The amplified signal from A1 is gated by G1 and in turn sets the FF. Assume, for the time, that G2 is low. The combination of the FF and One Shot 1 produces a minimum pulse to clock the counter-decoder for each positive *edge* at pin 13 which exceeds the voltage on pin 12. The width of this pulse is: $T_m = R_mC_m$. With this arrangement, the system will not respond to any pulse after the first edge and before the end of T_m. In effect the input is turned off for a period equal to T_m following the leading edge of each input pulse. The noise immunity of the decoder is thus enhanced by the ratio of T_m to the period between input pulses. Obviously T_m must be less than the shortest period between input pulses.

The counter is clocked and One Shot 2 is reset (capacitor C_s is discharged) each time the FF is set. When the FF is reset, C_s begins to charge up through R_s. The time constant $T_s = .85\ R_sC_s$ is normally much larger than the time between input pulses so that the output of One Shot 2 remains low until the last pulse of a given frame is received. Figure 1 shows the timing diagram for the decoder. After the last pulse in a frame (system synchronized) $\overline{Q}_o$ will go low and G2 will go high. The input is now disabled by G1 until One Shot 2 times out at which time G2 will go low. This connection serves two purposes:

(1) establishes synchronization in no more than one frame and

(2) prevents the counter-decoder from overflowing due to extra noise pulses in a given frame. Thus any noise pulses in a frame will only affect those channels after that pulse and only in that frame.

If fewer than 7 channels of input are used then $\overline{Q}_o$ is high after the last pulse and the counter-decoder is reset when One Shot 2 goes high.

Each channel has a totem pole output stage capable of sourcing 2mA and sinking 1mA.

The voltage regulator operates in two modes depending on the power supply voltage. If V_{CC} is greater than 5V, the voltage regulator acts as a series pass regulator with a nominal output voltage of 4.1V. When V_{CC} is less than 5V, the regulator acts as a dynamic decoupler where the bypass capacitor on pin 14 filters out line transients. The internal pass transistor acts like an emitter follower whose base is decoupled by the bypass capacitor. The value of capacitance will depend upon the degree of smoothing required and the amplitude of the line transients. If the regulator provides power for the radio receiver, this capacitor may have to be as large as 33μF. However if this is not done, 1μF should be sufficient.

B. DECODER DESIGN EQUATIONS

The design of the decoder's external circuitry is quite simple. The minimum pulse One Shot (#1) and the synchronization One Shot (#2) each have time periods given by:

$$T_m = R_mC_m$$

$$T_s = .85\ R_sC_s$$

respectively. The constraints on these time periods are: T_m < the minimum input pulse width or time between leading edges of the input and T_s > maximum input pulse width but T_s < the sync pause (time between last pulse in frame and first pulse of the following frame).

The design of the input amplifier biasing network depends upon a number of factors, including:

1. Pulse Polarity
2. Pulse Amplitude
3. Variations in Amplitude and Noise
4. Detection Threshold and Hysteresis Levels

For a very simple case, assume the input is a positive pulse train and the threshold of detection is desired to be 400mV without hysteresis. Figure 2 shows the input amplifier along with the associated biasing circuits. The resistors R_1 and R_2 set the voltage on pin 12, which should be between 2V to 5V.

$$V_{12} = V_R \frac{1}{1 + R_1/R_2}$$

The threshold is set by the voltage drop across R_3, that is, the decoder will not be triggered until the voltage on pin 13 exceeds the voltage on pin 12.

$$V_{threshold} = V_{12} - V_{13}$$

$$V_{threshold} = V_{12}\left(\frac{1}{1 + R_4/R_3}\right)$$

If we assume $V_R = 4.1V$ and let $V_{12} = 3V$ then

$R_1 = 1.1k$

$R_2 = 3.0k$

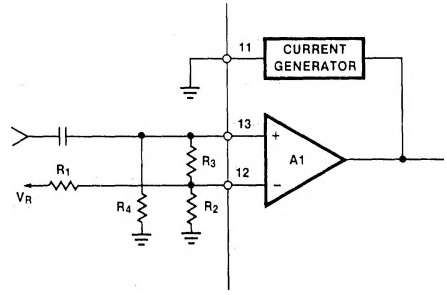


Figure 2. Input Amplifier Biasing NE5045

The threshold is then set to 400mV by setting

$R_4/R_3 = 6.5$

R_4 should be sufficiently large so as to not load the input signal. If we let $R_3 = 51k$ then $R_4 = 330k$. Figure 3 shows the external connections for a complete decoder. Note that this circuit does not have provisions for noise filtering or rejection of amplitude variations.

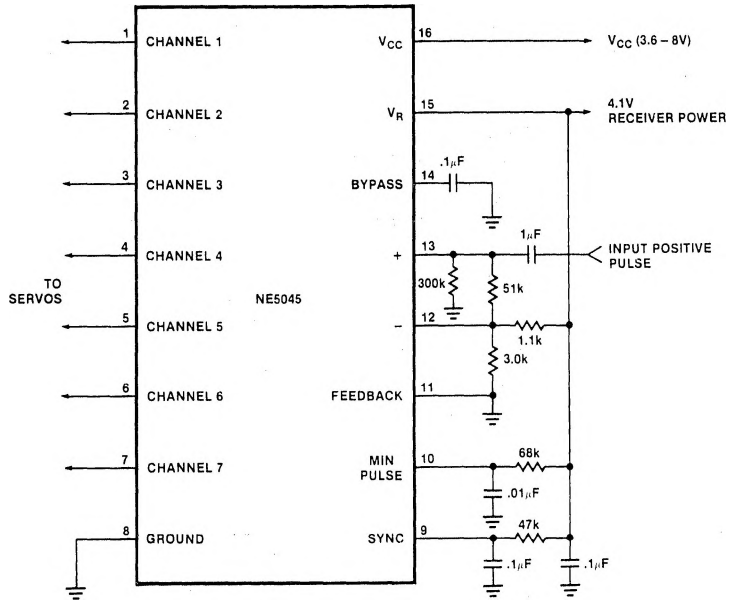


Figure 3. NE5045 Decoder External Connections
$T_m = .68ms$; $T_s = 4ms$, $V_{threshold} = 400mV$

***For additional information, consult the Applications Section.**