National Semiconductor

PRELIMINARY

# PAL10/10016PE8-3 (PLCC Only)
# 3 ns ECL ASPECT™ Programmable Array Logic

## General Description

The PAL10/10016PE8-3 is a member of the National Semiconductor 28-pin high speed ECL PAL® family. This device utilizes National Semiconductor's ASPECT (Advanced Single Poly Emitter Coupled Technology) process with a newly developed tungsten fuse technology to provide the highest-speed user-programmable replacements for conventional ECL SSI-MSI logic with significant chip-count reduction. The JEDEC fuse-map format and programming algorithm of this device is compatible with those of all prior ECL PAL products from National.

Programmable logic devices provide convenient solutions for a wide variety of applications—specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the shelf products.

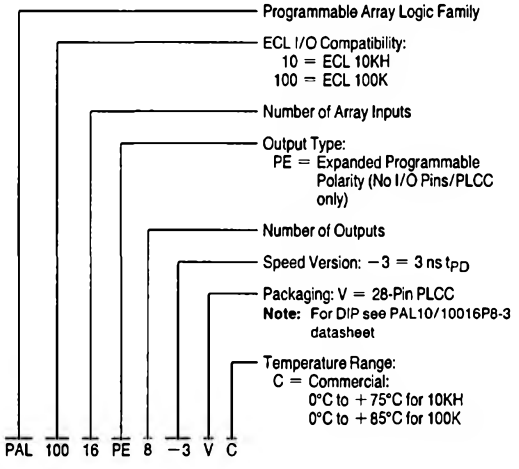
The PAL10/10016PE8-3 logic array has a total of 16 complementary input pairs, 64 product terms and 8 programmable polarity output functions. Each output function is the OR-sum of 8 product terms. Each product term is satisifed when all array inputs which are connected to it (via intact fuses) are in the correct state as defined by the equation for that product term. Each output function is provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by industry standard conventional TTL PLD programmers. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

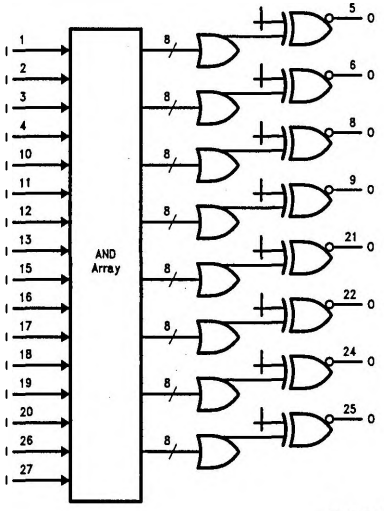
## Features

- High speed: $t_{PD}$ 3 ns max
- Full 28-pin function (all pins used)
- Programmable replacement for ECL logics
- Both 100K and 10 KH I/O compatible versions
- Eight output functions with programmable polarity
- Security fuse to prevent direct copying
- Fully supported by PLAN and other industrial software
- High density-high performance 28-pin PLCC package

## Ordering Information




## Block Diagram

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## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Temperature under Bias | −55°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| $V_{EE}$ Relative to $V_{CC}$ | −7V to +0.5V |
| Input Voltage | $V_{EE}$ to +0.5V |
| Output Current | −50 mA |
| Lead Temperature (Soldering, 10 Seconds) | TBD |

ESD Tolerance
$C_{ZAP}$ = 100 pF
$R_{ZAP}$ = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5028

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{EE}$ | Supply Voltage | 10KH | −5.46 | −5.2 | −4.94 | V |
| | | 100K | −4.80 | −4.5 | −4.20 | |
| T | Operating Temperature (Note) | 10KH | 0 | | +75 | °C |
| | | 100K | 0 | | +85 | |

## Electrical Characteristics Over Recommended Operating Conditions Output Load = 50Ω to −2.0V

| Symbol | Parameter | Conditions | | $T_A$ | Min | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | Guaranteed Input Voltage High for All Outputs | 10KH | 0°C<br>+25°C<br>+75°C | −1170<br>−1130<br>−1170 | −840<br>−810<br>−735 | mV |
| | | | 100K | 0°C to +85°C | −1165 | −880 | |
| $V_{IL}$ | Low Level Input Voltage | Guaranteed Input Voltage Low for All Inputs | 10KH | 0°C<br>+25°C<br>+75°C | −1950<br>−1950<br>−1950 | −1480<br>−1480<br>−1450 | mV |
| | | | 100K | 0°C to +85°C | −1810 | −1475 | |
| $V_{OH}$ | High Level Output Voltage | $V_{IN}$ = $V_{IH}$ Max or $V_{IL}$ Min | 10KH | 0°C<br>+25°C<br>+75°C | −1020<br>−980<br>−920 | −840<br>−810<br>−735 | mV |
| | | | 100K | 0°C to +85°C | −1025 | −880 | |
| $V_{OL}$ | Low Level Output Voltage | $V_{IN}$ = $V_{IH}$ Max or $V_{IL}$ Min | 10KH | 0°C<br>+25°C<br>+75°C | −1950<br>−1950<br>−1950 | −1630<br>−1630<br>−1600 | mV |
| | | | 100K | 0°C to +85°C | −1810 | −1620 | |
| $I_{IH}$ | High Level Input Current | $V_{IN}$ = $V_{IH}$ Max | 10KH | 0°C<br>+75°C | | 220 | μV |
| | | | 100K | 0°C to +85°C | | | |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = $V_{IH}$ Min | 10KH | 0°C<br>+75°C | 0.5 | | μV |
| | | | 100K | 0°C to +85°C | | | |
| $I_{EE}$ | Supply Current | $V_{EE}$ = Min All Inputs and Outputs Open | 10KH | 0°C to +75°C | −220 | | mA |
| | | | 100K | 0°C to +85°C | | | |

**Note:** Operating temperatures for circuits in PLCC packages are specified as ambient temperatures ($T_A$) with circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

## Switching Characteristics

Over Recommended Operating Conditions, Output load: $R_L$ = 50Ω to −2.0V, $C_L$ = 5 pF to GND

| Symbol | Parameter | Measured Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $t_{PD}$ | Input to Output | Measured at Threshold Points (Note 1) | | 3.0 | ns |
| $t_r$ | Output Rise Time | Measured between 20% and 80% Points | 0.25 | 1.25 | ns |
| $t_f$ | Output Fall Time | | 0.25 | 1.25 | ns |

**Note 1:** All AC Measurements are to be made from Threshold Point.

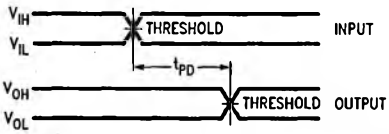
$V_{IH}$ = Threshold + 400 mV

$V_{IL}$ = Threshold − 400 mV

$$\text{Threshold} = \frac{V_{IH_{Min}} + V_{IL_{Max}}}{2}$$

| Part | Temp | $V_{IN_{Min}}$ | $V_{IL_{Max}}$ | Threshold | $V_{IH}$ | $V_{IL}$ |
|---|---|---|---|---|---|---|
| 10 kH | 0°C | −1170 | −1480 | −1325 | −925 | −1725 |
| 10 kH | 25°C | −1130 | −1480 | −1300 | −900 | −1700 |
| 10 kH | 75°C | −1070 | −1450 | −1260 | −860 | −1660 |
| 100k | All | −1165 | −1475 | −1300 | −900 | −1700 |

## Timing Measurements

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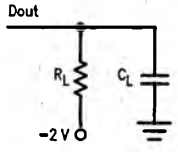
## Test Load

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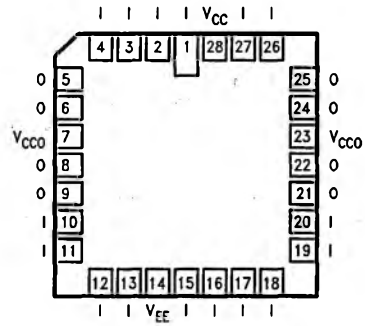
## Connection Diagram

**PLCC**

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**Top View**

**Order Number PAL1016PE8-3/PAL10016PE8-3**
**See NS Package Number V28A**

## Functional Testing

As with all field-programmable devices, the user of the ECL PAL devices provides the final manufacturing step. While National's PAL devices undergo extensive testing when they are manufactured, their logic function can be fully tested only after they have been programmed to the user's pattern.

To ensure that the programmed PAL devices will operate properly in your system, National Semiconductor (along with most other manufacturers of PAL devices) strongly recommends that devices be functionally tested before being installed in your system. Even though the number of postprogramming functional failures is small, testing the logic function of the PAL devices before they reach system assembly will save board debugging and rework costs. For more information about the functional testing of PAL devices, please refer to National Semiconductor's Application Note #351 and the *Programmable Logic Design Guide*.

## Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be downloaded into a large variety of programming equipment. Many software packages and programming units support a large variety of programmable logic products as well. The PLAN software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

A detailed logic diagram showing all JEDEC fuse-map addresses for the PAL10/10016PE8-3 is provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the ECL PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

## Programmer Support

| | | |
|---|---|---|
| Advin Systems | Sailor PAL | V8.40 |
| Data I/O | Unisite 40 | V2.7 |
| International Microsystems | ECL-2, ECL-1 | |
| Logical Devices | Allpro | V1.48C |
| | Palpro 2X | V4.0 |
| Stag Microsystems | ZL30A | V31 |

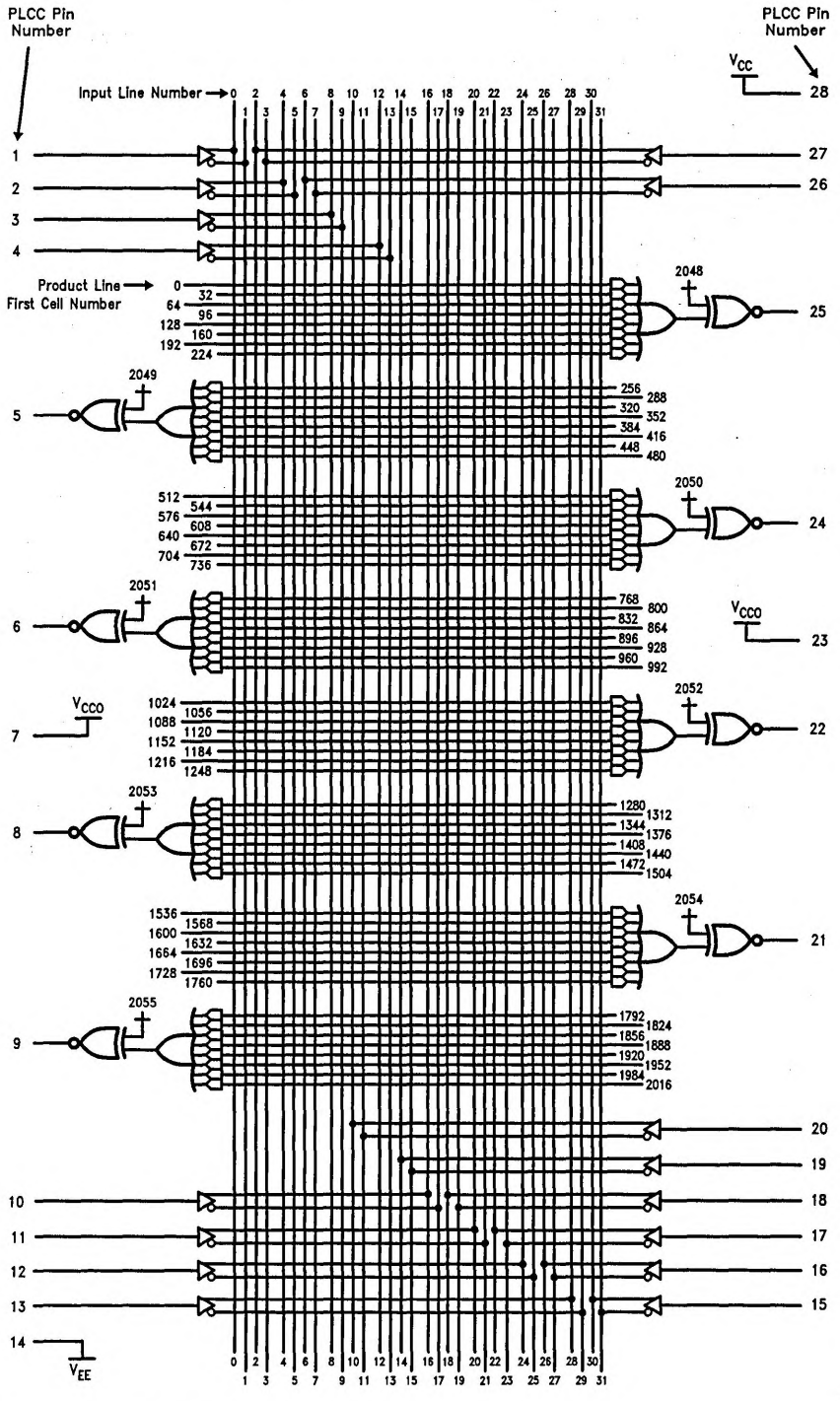
## Programming

Most programmers listed below are able to directly program the 28-lead PLCC package. If programming from a DIP socket the following adapter wiring is required:

| PLCC Pin | DIP Pin |
|---|---|
| 1 | No Connect |
| 2 | 1 |
| 3 | 2 |
| 4 | 3 |
| 5 | 4 |
| 6 | 5 |
| 7 | 6 |
| 8 | 7 |
| 9 | 8 |
| 10 | No Connect |
| 11 | 9 |
| 12 | 10 |
| 13 | 11 |
| 14 | 12 |
| 15 | No Connect |
| 16 | 13 |
| 17 | 14 |
| 18 | 15 |
| 19 | 16 |
| 20 | No Connect |
| 21 | 17 |
| 22 | 18 |
| 23 | 19 |
| 24 | 20 |
| 25 | 21 |
| 26 | 22 |
| 27 | 23 |
| 28 | 24 |

PLCC pins 1, 10, 15 and 20 are not connected to the DIP pins because these are the additional ECL inputs. If using such an adaptor, a 0.1 $\mu$F capacitor should be added from PLCC pin 23 to PLCC pin 14.

# Logic Diagram—PAL1016PE8-3/PAL10016PE8-3

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JEDEC logic array cell number = product line first cell number + input line number