Fractional-N Frequency Synthesizer for DAB Tuner

Description

The U2733B-D is a monolithic integrated fractional-N frequency synthesizer circuit fabricated with TEMIC's advanced UHF5S technology. Designed for applications in DAB receivers, it controls a VCO to synthesize frequencies in the range of 70 MHz to 500 MHz in a 16-kHz raster; four different reference divide factors can be selected. The lock status of the phase detector is indicated at a special output pin. Four switching outputs can be addressed. A reference signal is generated by an on-chip reference oscillator. A frequency doubler provides an output signal at twice the frequency of the reference oscillator. Two D/A converters at a resolution of 8 bit provide a digitally controllable output voltage. All functions of this IC are controlled by an I^{2}C bus.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Microprocessor-controlled via I^{2}C bus
- 4 addresses selectable
- Reference oscillator
- Reference frequency doubler (open-collector output)
- Four reference divide factors selectable:
  1024, 1120, 1152, 1536 effectively
- Programmable 15-bit counter
  1:2048 to 1:32767 effectively
- Tristate phase detector with programmable charge pump
- Superior phase-noise performance
- Deactivation of tuning output programmable
- 4 switching outputs (open collector)
- 2 D/A converters (resolution: 8 bit)
- Lock-status indication (open collector)

Block Diagram

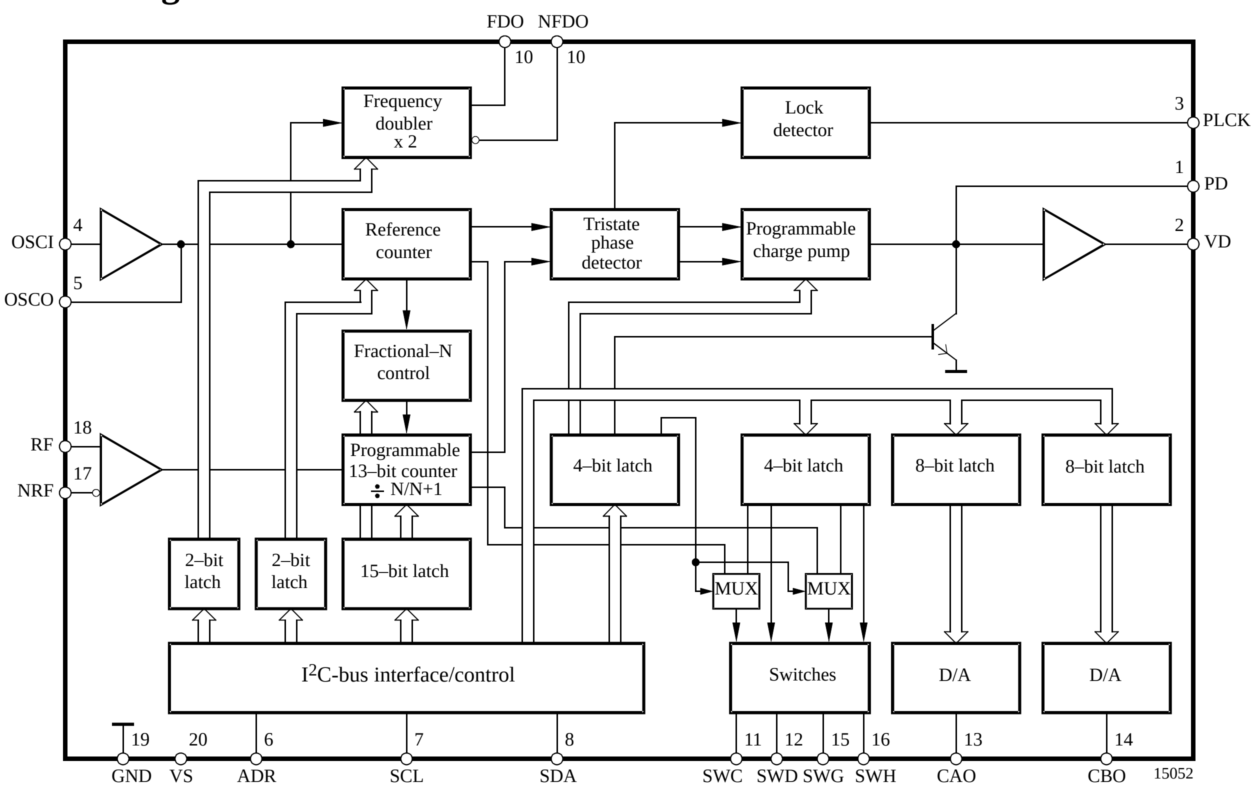


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2733B-DFS	SSO20	
U2733B-DFSG1	SSO20	Taped and reeled according to IEC 286–3

Pin Description

Figure 2. Pinning

Pin	Symbol	Function
1	PD	Tristate charge pump output
2	VD	Active filter output
3	PLCK	Lock-indicating output (open collector)
4	OSCI	Input of reference oscillator/ buffer
5	OSCO	Output of reference oscillator/ buffer
6	ADR	Address selection
7	SCL	Clock (I^2C)
8	SDA	Data (I^2C)
9	NFDO	Frequency-doubler output (inverted, open collector)
10	FDO	Frequency-doubler output (open collector)
11	SWC	Switching output (open collector)
12	SWD	Switching output (open collector)
13	CAO	Output of D/A converter A
14	CBO	Output of D/A converter B
15	SWG	Switching output (open collector)
16	SWH	Switching output (open collector)
17	NRF	RF input (inverted)
18	RF	RF input
19	GND	Ground
20	VS	Supply voltage

Functional Description

The U2733B-D is a low-power fractional-N frequency synthesizer designed for applications in DAB receivers. Its RF operation range is 70 MHz to 500 MHz. As shown in the block diagram in figure 1, the device includes a reference oscillator, a reference divider, an input buffer for the RF divider, a programmable RF divider using fractional-N technique, a tristate phase detector, a programmable charge pump, four switching outputs, a frequency doubler for the reference signal, two D/A converters at a resolution of 8 bit and a control unit. The control unit has to be accessed by a microcontroller via an I^2C bus. The device is mounted in an SSO20 package. An appropriate application circuit is given in figure 8.

The most striking feature of this circuit is the use of a special phase-noise shaping technique based on the fractional-N principle which concentrates the phase detector's phase-noise contribution to the spectrum of the controlled VCO at frequency positions where it does not damage the quality of the received DAB signal. A special property of the transmission technique which is used in DAB is that the phase-noise weighting function (which measures the influence of the LO's phase noise to the phase information of the coded signal in a DAB receiver) has zeros, i.e., if phase noise is concentrated in the position of such zeros as discrete lines, the DAB signal is not impaired as long as these lines do not exceed a certain limit. For DAB mode I, this phase-noise weighting function is shown in figure 3.

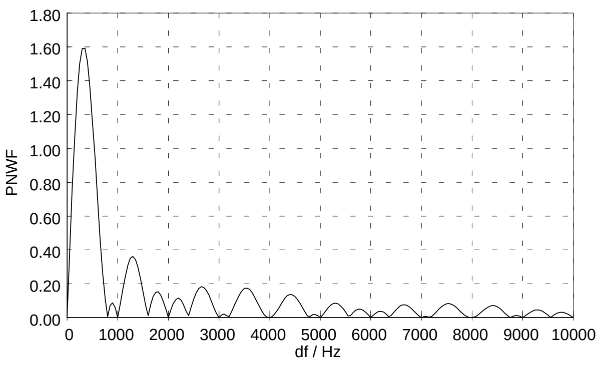


Figure 3.

It is important to realize that this function shows zeros in all distances from the center line which are multiples of the carrier spacing. The technique of concentrating the phase noise in the positions of such zeros is protected by a patent.

In this circuit, the phase detector is operated at a frequency which is four times the desired frequency raster spacing (e.g. 16 kHz in case of DAB) and the well-known fractional-N technique is used to synthesize the raster. As a result of this technique, spurious in the VCO's frequency spectrum (see figure 10) occur not only in multiples of the phase detector's input comparison frequency (64 kHz) but also in multiples of the raster frequency (16 kHz). As described above, for all DAB modes these spurious are placed in spectral positions where the phase-noise weighting function is zero. Therefore, no measures are necessary to suppress these lines. The phase-noise performance of this circuit is demonstrated in figure 9.

Reference Oscillator

An on-chip oscillator generates the reference signal which is fed to the reference divider. By applying a crystal externally, as shown in figure 6, this oscillator generates a highly stable reference signal. If an external reference signal is available, the oscillator can be used as an input buffer. In such an application as that shown in figure 7, the reference signal has to be applied to the Pin OSCI and the Pin OSCO must be left open.

Reference Divider

Four different scaling factors, SF_{ref}, of the reference divider can be selected by means of the bits RD1 and RD2 in the I^2C-bus instruction code: 256, 280, 288, and 384. Starting from a reference oscillator frequency of 16.384 MHz/ 17.92 MHz/ 18.432 MHz/ 24.576 MHz, these scaling factors provide a frequency raster of 64 kHz. By changing the division ratio of the main divider from N to N+1 in an appropriate way (fractional-N technique), this frequency raster is interpolated to deliver a frequency spacing of 16 kHz according to the DAB specification. So, effectively, the reference divide factors 1024, 1120, 1152 and 1536 can be selected. By setting the I^2C-bus bit 'T', a test signal representing the divided input signal can be monitored at the switching output SWC.

Preliminary Information

Main Divider

The main divider consists of a fully programmable 13-bit divider which defines a division ratio N. The applied division ratio is either N or N+1 according to the setting of a special control unit. Generally speaking, the scaling factors SF = N+k/4 can be selected where k = 0, 1, 2, 3. In this way, VCO frequencies

$$f_{VCO} = 4 \times (N+k/4) \times f_{ref}/(4 \times SF_{ref})$$

can be synthesized starting from a reference frequency, $f_{ref.}$. If we define $SF_{eff} = 4 \times N+k$ and $SF_{ref,eff} = 4 \times SF_{ref}$ we have

$$f_{VCO} = SF_{eff} \times f_{ref} / SF_{ref,eff},$$

where SF_{eff} is defined by 15 bits. In the following this circuit is described in terms of SF_{eff} and $SF_{ref,eff}$. SF_{eff} has to be programmed via the I^2C-bus interface. An effective scaling factor from 2048 to 32767 can be selected. By setting of the I^2C-bus bit T a test signal representing the divided input signal can be monitored at the switching output SWF.

When the supply voltage is switched on both the reference divider and the programmable divider are kept in RESET state till a complete scaling factor is written onto the chip. Changes in the setting of the programmable divider become active when the corresponding I^2C-bus transmission is completed. An internal synchronization procedure ensures that such changes do not become active while the charge pump is sourcing or sinking current at its output pin. This behavior allows smooth tuning of the output frequency without disturbing the controlled VCO's frequency spectrum.

Phase Comparator and Charge Pump

The tristate phase detector causes the charge pump to source or to sink current at the output Pin PD depending on the phase relation of its input signals which are provided by the reference and the main divider respectively. Four different values of this current can be selected by means of the I^2C-bus bits I50 and I100. By means of this option, for example, changes of the loop characteristics due to the variation of the VCO gain as a function of the tuning voltage can be reduced. The charge pump current can be switched off using the I^2C-bus bit TRI. A change in the setting of the charge pump current becomes active when the corresponding I^2C-bus transmission is completed. As described for the setting of the scaling factor of the programmable divider, an internal synchronization procedure ensures that such changes don't become active while the charge pump is sourcing or sinking current at its output pin. This behavior allows a change in the charge pump current without disturbing the controlled VCO's frequency spectrum.

A high gain amplifier (output pin: VD) which is implemented in order to construct a loop filter, as shown in the application circuit, can be switched off by means of the I^2C-bus bit OS.

An internal lock detector checks if the phase difference of the input signals of the phase detector is smaller than approximately 250 ns in seven subsequent comparisons. If phase lock is detected the open collector output Pin PLCK is set HIGH (logical value!). It should be noted that the output current of this pin must be limited by an external circuit as it is not limited internally. If the I^2C-bus bit TRI is set HIGH the lock detector function is deactivated and the logical value of the PLCK output is undefined.

Switching Outputs

Four switching outputs, controlled by the I^2C-bus bits SWC, SWD, SWG, SWH, can be used for any switching task on the front-end board. The currents of these outputs are not limited internally. They have to be limited by external circuitry.

Frequency Doubler

An internal frequency doubler provides a signal at twice the frequency of the reference signal appearing at the input Pins REF and NREF. If the I^2C-bus bit OFD = HIGH, the current of its open collector outputs FDO and NFDO is doubled. By means of the I^2C-bus bit OFD, the frequency-doubler function can be switched off.

As shown in figure 11 (Integration in TEMIC DAB Receiver Concept), the output signal of the frequency doubler can be used to construct the LO signal of the IF circuit (U2759B).

D/A Converters

Two D/A converters, A and B, offer the possibility to generate two output voltages at a resolution of 8 bits. These voltages appear at the output Pins CAO and CBO. The converters are controlled via the I^2C-bus interface by means of the control bits CA0, ..., CA7 and CB0, ..., CB7 respectively as described in the chapter 'I^2C-Bus Instruction Codes'. The output voltages are defined as

$$V_{CAO} = V_M /128 \times \sum CAj \times 2^j, \quad j = 0, .., 7$$

$$V_{CBO} = V_M /128 \times \sum CBj \times 2^j, \quad j = 0, .., 7$$

where V_M = 2.5 V nominally. Due to the rail-to-rail outputs of these converters, virtually the full voltage range from 0 to 5 V can be used. A common application of these converters is the digital synthesis of control signals for tuning of preselectors.

I^2C-Bus Interface

Via its I^2C-bus interface, various functions can be controlled by a microprocessor. These functions are outlined in the following chapter 'I^2C-Bus Instruction Codes' and 'I^2C-Bus Functions'. The programming information is stored in a set of internal registers. By means of the ADR pin, four different I^2C-bus addresses can be selected as described in the chapter 'Electrical Characteristics'. In figure 4, the I^2C-bus timing parameters are explained, figure 5 shows a typical I^2C-bus pulse diagram.

Table 1. I^2C-Bus Instruction Codes

Description	MSB							LSB
Address byte	1	1	0	0	0	AS1	AS2	0
Divider byte 1	0	RD1	RD2	X	X	n_{14}	n_{13}	n_{12}
Divider byte 2	X	X	n_{11}	n_{10}	n_9	n_8	n_7	n_6
Divider byte 3	X	X	n_5	n_4	n_3	n_2	n_1	n_0
Control byte 1	1	1	0	OS	T	TRI	I100	I50
Control byte 2	OFD	2IFD	SWC	SWD	X	X	SWG	SWH
Control byte 3	X	0	0	0	0	0	0	0
Converter byte 1	1	0	X	X	X	X	X	X
Converter byte 2	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Converter byte 3	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0

I^2C-Bus Functions

AS1, AS2 define the I^2C-bus address

RD1, RD2 define the effective scaling factor of the reference divider:

RD1	RD2	Effective Scaling Factor
0	0	1120
1	0	1152
0	1	1024
1	1	1536

n_i effective scaling factor (SF_{eff}) of the main divider

$SF_{eff} = SUM(n_i\ 2^i)$

OS OS = HIGH switches off the tuning output

T for T = HIGH, reference signals describing the output frequencies of the reference divider and programmable divider are monitored at SWC (reference divider) and SWF (programmable divider)

TRI TRI = HIGH switches off the charge pump

CAi, CBi define the setting of the two D/A converters A and B (i = 0, ..., 7)

I50, I100 define the charge pump current

I50	I100	Charge-Pump Current (nominal) / µA
LOW	LOW	50
HIGH	LOW	102
LOW	HIGH	151
HIGH	HIGH	203

OFD OFD = HIGH switches off the frequency doubler

2IFD 2IFD = HIGH doubles the frequency doubler output current

SWa SWa = HIGH switches on the output current

I^2C-Bus Data Transfer

Format:

START – ADR – ACK – <instruction set> – STOP

The <instruction set> consists of a sequence of divider bytes, control bytes and converter bytes each followed by ACK. Divider byte i must be followed by divider byte i+1 (control byte 1 if i = 3) or the instruction set must be finished. Control bytes and converter bytes have to be handled accordingly.

Examples:

START – ADR – ACK – DB1 – ACK – DB2 – ACK – DB3 – ACK – CTB1 – ACK – CTB2 – ACK – CTB3 – ACK – CVB1 – ACK – CVB2 – ACK – CVB3 – ACK – STOP

START – ADR – ACK – CB1 – ACK – CB2 – ACK – STOP

However:

START – ADR – ACK – DB1 – ACK – CB1 –ACK – STOP is not allowed.

Description:

START	start condition
STOP	stop condition
ACK	acknowledge
ADR	address byte
DBi	divider byte i (i=1,2,3)
CTBi	control byte i (i=1,2,3)
CVBi	converter byte i (i=1,2,3)

I^2C-Bus Timing

The values of the drawn periods are specified in the section ‘Electrical Characteristics’. More detailed information can be taken from Application Note 1.0 (I^2C-Bus Description). Please note: due to the I^2C-bus specification, the MSB of a byte is transmitted first, the LSB last.

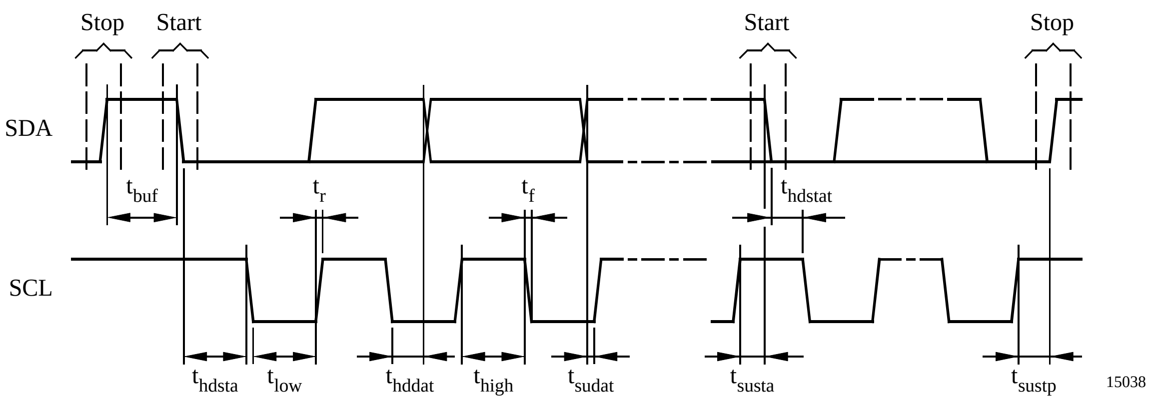


Figure 4. I^2C-bus timing

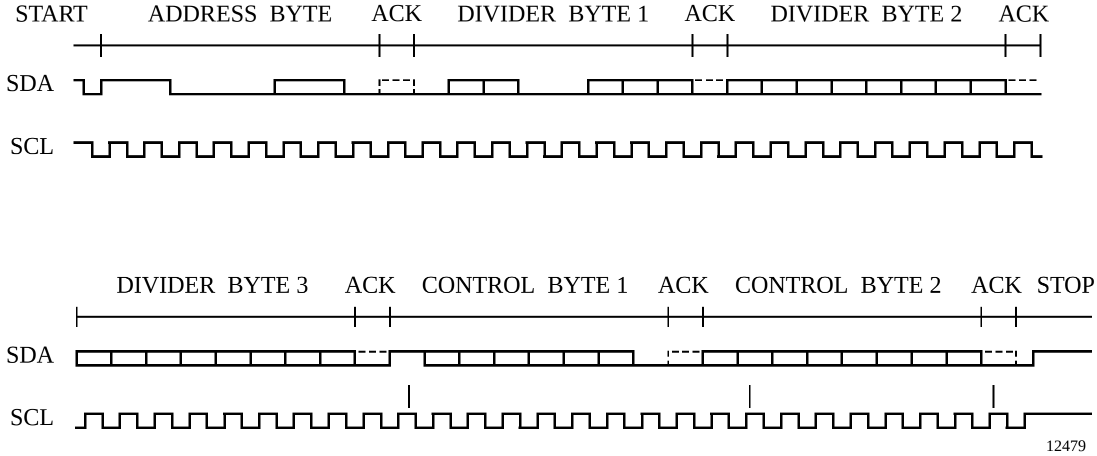


Figure 5. Typical I^2C-bus pulse diagram

Absolute Maximum Ratings

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_S	–0.3		+5.5	V
RF input voltage (AC)	Pins 17 and 18	V_{RF}, V_{NRF}			1	V_{pp}
Reference input voltage (AC)	Pin 4	V_{OSCI}			1	V_{pp}
I^2C-bus input / output voltage	Pins 7 and 8	V_{SCL}, V_{SDA}	–0.3		V_S	V
SDA output current	Pin 8	I_{SDA}			5	mA
Address select voltage	Pin 6	V_{ADR}	–0.3		5.5	V
Switch output voltage, open collector	Pins 11, 12, 15 and 16	V_{SWa}	–0.3		5.5	V
Switch output current, open collector		I_{SWa}	4			mA
PLCK output voltage	Pin 3	V_{PLCK}	–0.3		5.5	V
PLCK output current	Pin 3	I_{PLCK}			0.5	mA
Frequency doubler output, open collector	Pins 9 and 10	V_{FDO}, V_{NFDO}	V_S –1		5.5	V
Junction temperature		T_j			125	°C
Storage temperature		T_{stg}	–40		+125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	140	K/W

Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	V_S	4.5 to 5.5	V
Ambient temperature range	T_{amb}	–40 to +85	°C

Electrical Characteristics

Test conditions: V_S = 5 V, T_{amb} = 25°C (if not otherwise stated)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current	SW_a = LOW, TRI = LOW, PLCK = LOW, OS = LOW, I50 = HIGH, I100 = HIGH, OFD = LOW, 2IFD = LOW	I_S	14.5	18.1	21.7	mA
	SW_a = LOW, TRI = LOW, PLCK = LOW, OS = LOW, I50 = HIGH, I100 = HIGH, OFD = HIGH, 2IFD = LOW	I_{SO}		16.2		mA
Effective scaling factor of programmable divider		SF_{eff}	2048		32767	
Effective scaling factor of reference divider	RD1 = LOW, RD2 = LOW RD1 = HIGH, RD2 = LOW RD1 = LOW, RD2 = HIGH RD1 = HIGH, RD2 = HIGH	$SF_{ref,eff}$		1120 1152 1024 1536		
Tuning step	17.920 MHz/ 18.432 MHz/ 16.384MHz/ 24.576MHz reference frequency	f_{rast}		16		kHz

Electrical Characteristics (continued)

Test conditions: V_S = 5 V, T_{amb} = 25°C (if not otherwise stated)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
RF input	**Pins 17 and 18**					
Input frequency range	V_S = 4.5 V, T_{amb} = 20°C	f_{rf}	70		500	MHz
Input sensitivity		V_{rfs}		10	20	mV_{rms}
Maximum input signal		V_{rfmax}			300	mV_{rms}
Input impedance	Differential	Z_{rf}		200		Ω
VSWR		$VSWR_{rf}$		2		
REF input	**Pin 4**					
Input frequency range	V_S = 4.5 V, internal oscillator overdriven	f_{ref}	5		30	MHz
Input sensitivity	Internal oscillator overdriven	V_{refs}			50	mV_{rms}
Maximum input signal	Internal oscillator overdriven	V_{refmax}			300	mV_{rms}
Input impedance	Single ended	Z_{ref}		2 || 2.5		kΩ/pF
Phase detector	**Pin 1**					
Charge-pump current	I100 = HIGH, I50 = HIGH	I_{PD4}	± 160	± 203	± 240	µA
	I100 = HIGH, I50 = LOW	I_{PD3}	± 120	± 151	± 180	µA
	I100 = LOW, I50 = HIGH	I_{PD2}	± 80	± 102	± 120	µA
	I100 = LOW, I50 = LOW	I_{PD1}	± 40	± 50	± 60	µA
	TRI = HIGH	$I_{PD,tri}$			± 100	nA
Effective phase noise *)	I_{PD} = 203 µA	L_{PD}		–163		dBc/Hz
Lock indication	**Pin 3**					
Leakage current	V_{PLCK} = 5.5 V	$I_{PLCK,L}$			10	µA
Saturation voltage	I_{PLCK} = 0.5 mA	$V_{PLCK,sat}$			0.5	V
Frequency doubler	**Pins 9 and 10**					
Output current	V_{FDO} = V_S, V_{NFDO} = V_S, 2IFD = LOW	I_{FDOL}, I_{NFDOL}	0.4	0.5	0.6	mA_{pp}
	V_{FDO} = V_S, V_{NFDO} = V_S, 2IFD = HIGH	I_{FDOH}, I_{NFDOH}	0.8	1.0	1.2	mA_{pp}
Minimum output voltage	V_S = 5 V	V_{FDO}, V_{NFDO}	4			V
Switches	**Pins 11, 12, 15 and 16**					
Leakage current	V_{SWa} = 5.5 V	$I_{SW,L}$			10	µA
Saturation voltage	I_{SWa} = 4 mA	$V_{SW,sat}$			0.5	V
Address selection	**Pin 6**					
AS1 = 0, AS2 = 0			0		0.1 V_S	V
AS1 = 0, AS2 = 1				open		
AS1 = 1, AS2 = 0			0.4 V_S		0.6 V_S	V
AS1 = 1, AS2 = 1			0.9 V_S		V_S	V

*) The phase detector's phase-noise contribution to the VCO's frequency spectrum refer to the operating frequency of the phase detector divided by 4 according to the fractional-N technique (regularly: 16 kHz).

Electrical Characteristics (continued)

Test conditions: V_S = 5 V, T_{amb} = 25°C (if not otherwise stated)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
D/A converters	**Pins 13 and 14**					
Output voltage	CA7 = HIGH, CA0 ... CA6 = LOW, CB7 = HIGH, CB0 ... CB6 = LOW	V_M	2.4	2.5	2.6	V
Variation of V_M	V_S = 4.5 to 5.5 V	ΔV_{MVS}	–15		15	mV
	T_{amb} = –40 to +85°C	ΔV_{Mtemp}		±15		mV
Dynamic range	$\|V_{CAO} - n\ V_M/128\| \le 40$ mV, $\|V_{CBO} - m\ V_M/128\| \le 40$ mV, $n = \sum CAj \times 2^j$, $m = \sum CBj \times 2^j$	V_{LL}, V_{UL}	0.5		4.5	V
Maximum output current	$\|\Delta V_{CAO,CBO}\| \le 10$ mV, $0.5\ V \le V_{CAO,CBO} \le 4.5\ V$	I_{CAOmax}, I_{CBOmax}		20		µA
I²C bus	**Pins 7 and 8**					
Input voltage SCL/SDA	HIGH	V_H	3		5.5	V
	LOW	V_L			1.5	V
Output voltage SDA (open collector)	I_{SDA} = 2 mA, SDA = LOW				0.4	V
SCL clock frequency		f_{SCL}	0.1		100	kHz
Rise time (SCL, SDA)		t_r			1	µs
Fall time (SCL; SDA)		t_f			300	ns
Time before new transmission can start		t_{buf}	4.7			µs
SCL HIGH period		t_{high}	4			µs
SCL LOW period		t_{low}	4.7			µs
Hold time START		t_{hdsta}	4			µs
Set-up time START		t_{susta}	4.7			µs
Set-up time STOP		t_{sustp}	4.7			µs
Hold time DATA		t_{hddat}	0			µs
Set-up time DATA		t_{sudat}	250			ns

Application Circuits of Reference Oscillator

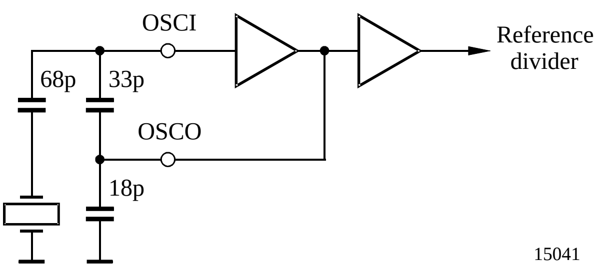


Figure 6. Oscillator operation

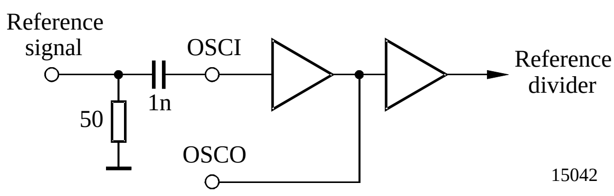


Figure 7. Oscillator overdriven

Application Circuit

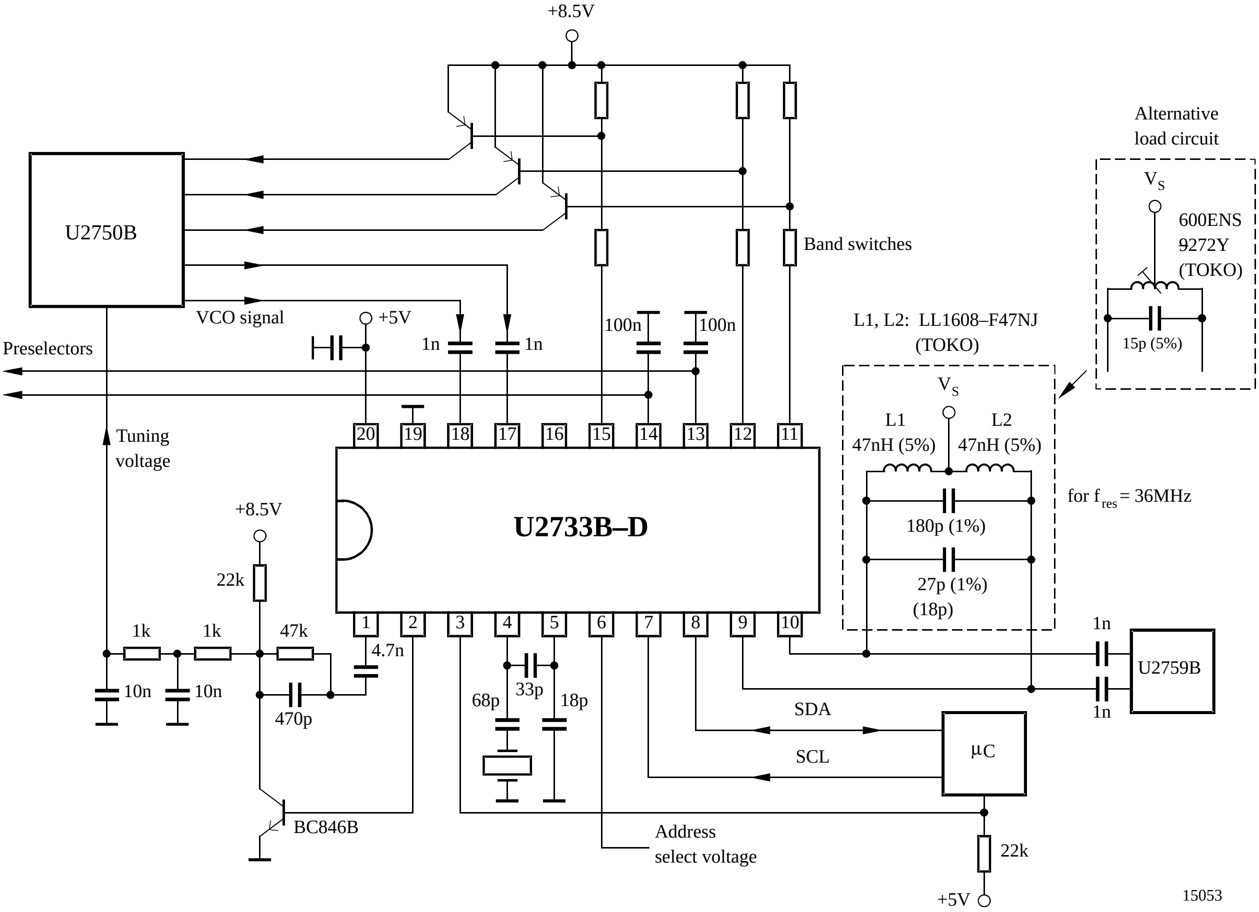


Figure 8.

Phase Noise Performance

(Example: SF_{eff} = 16899, $SF_{ref,eff}$ = 1120, f_{ref} = 17.92 MHz, I_{PD} = 200 A, spectrum analysis: HP70000, as application circuit above)

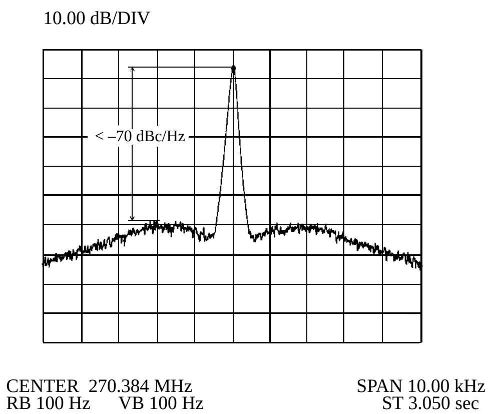


Figure 9.

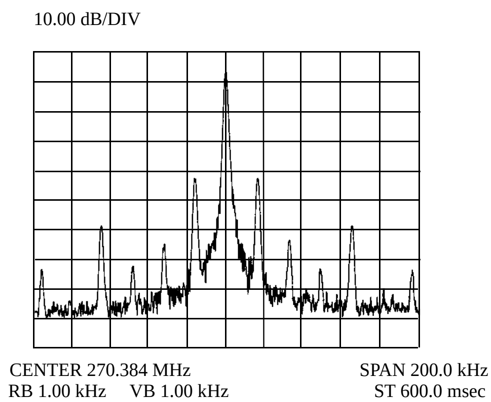


Figure 10.

Integration in TEMIC DAB Receiver Concept

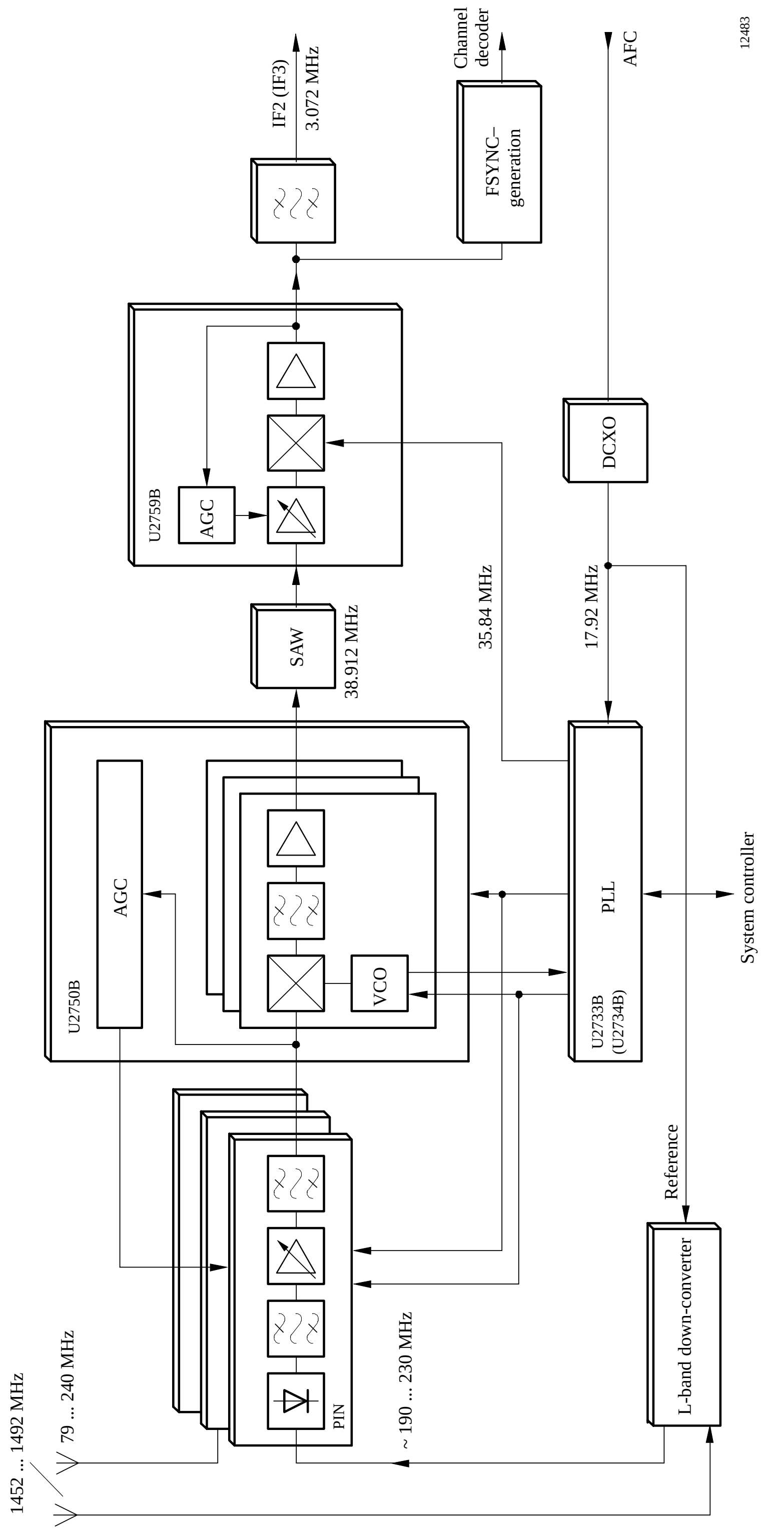
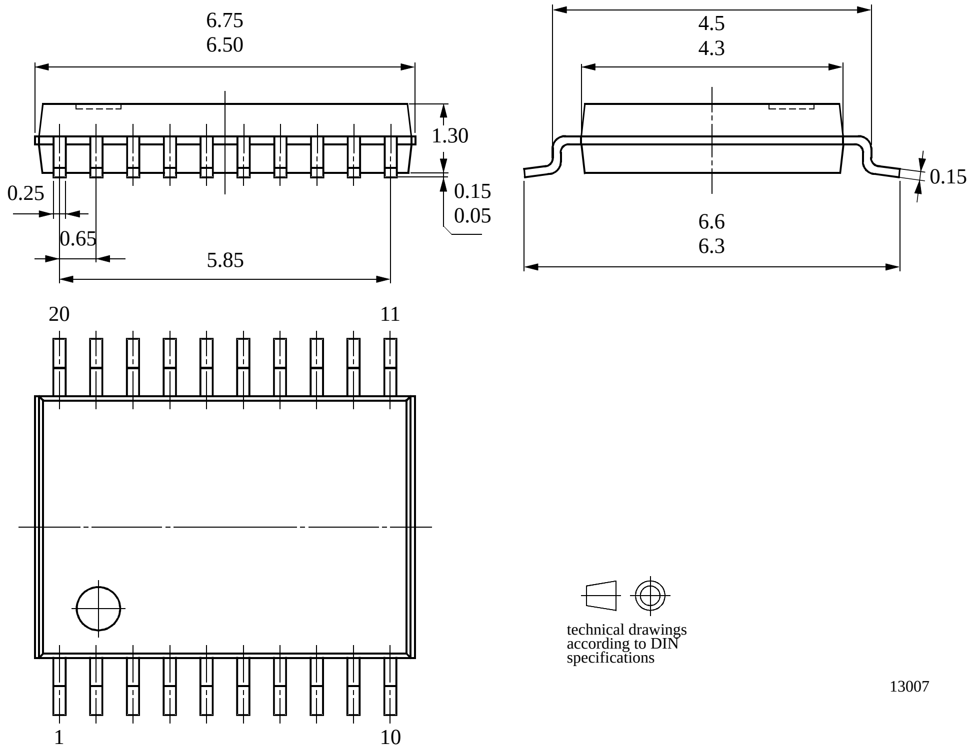


Figure 11. DAB receiver front end

Package Information

Package SSO20
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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